DESIGN OF A DISCRETE 64 CHANNEL NERVE RECORDER

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ABSTRACT

Injuries which lead to the damage of peripheral nerve can result in loss of motor function or sensory feedback. In severe cases, the damaged nerves do not regenerate leading to permanent disability. A possible solution lies in creating a neural link between the nerve and muscle thus bypassing the damaged portions totally. Such a system would require the recording, conditioning and interpreting of action potentials from the nerve sites using special electrodes. The objective of this project is to design and implement a 64-channel peripheral nerve recording system using discrete components. A novel design using a more efficient multiplexing algorithm was used to reduce the size, cost and power consumption of the system while still being able to provide a bandwidth of 30 kHz per recording channel. The drawback of this design is a degraded CMRR of 37.4dB at 50Hz. To make up for the low CMRR, a more aggressive low frequency cut off was adopted.

Finally, an input referred noise of 2μVrms for each channel was achieved by the use of low noise amplifiers. The bandwidth a channel was shown to be from 1 kHz to 10 kHz with a peak gain of 59.25dB at 3 kHz. Also, an estimate of the power required for a full 64 channel system was calculated to be 1.356W.

ACKNOWLEDGEMENTS

I would like to thank my two supervisors, Associate Professor Xu Yong Ping and Associate Professor Yen Shih Cheng for their patience and guidance throughout the project. Also, I would especially like to thank Ng Kian Ann for his invaluable help and advice on the multiplexing algorithm and many other areas.

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LIST OF SYMBOLS AND ABBREVIATIONS

DAQ Data Acquisition Unit

PNS Peripheral Nervous System

CNS Central Nervous System

FES Functional Electrical Stimulation

CAP Compound Action Potential

CHAPTER 1

INTRODUCTION

1.1 BACKGROUND

Peripheral Nervous System (PNS) and Nerves

The peripheral nervous system (PNS) is a collection of neuronal cells whose cell bodies are located in the spine and whose axons extend through peripheral nerves and terminate in certain sensory receptors or in neuromuscular junctions [1]. The PNS interfaces the central nervous system (CNS) to the skeletal muscles and sense receptors by transmitting information from sensory receptors to the CNS for sensing and transmitting information from the CNS to the skeletal muscles for reacting.

Such information is transmitted via electrochemical processes along a cable-like bundle of axons called the nerve. The peripheral nerve consists of both sensory and motor axons which are grouped into fascicles by an insulating perineurium; several fascicles are grouped together and surrounded by an insulating epineurium to form the peripheral nerve. It should be noted that neurons even within fascicles are grouped not according to their function (motor or sensory), but according to their destination. As one moves towards the spine, fascicles tend to fuse. Therefore, it is not possible to record or recruit fascicles based on their function [2].

Nerve Action Potentials

The resting potential of a cell is in the order of -50 to -100mV measured from the inside of the cell with respect to the outside [3]. When the cell membrane reaches a minimum threshold voltage by extracellular stimulation or otherwise, the cell membrane begins to depolarize, the influx of positive sodium ions increases the membrane potential further to about 40mv. Following this, the membrane quickly repolarizes to bring the membrane back to resting potential. There is a short period of time immediately after repolarization when the membrane drops below resting potential; this is known as the refractory period where further stimulation will not excite the cell, for example, a stimulus pulse applied 5ms after the first does not generate an action potential, but one applied after 10ms does [4]. The depolarization, repolarization and refractory period make up an action potential which is the signal of interest in recording systems such as the one described in this project.

Peripheral Nerve Injury, Functional Electrical Stimulation and Neuroprostheses

Injuries which lead to the severing of connections in the peripheral nerve would result in loss of motor function (if motor neurons are severed) or loss of sensory feedback (if sensory neurons are severed). A possible solution is presented in the field of functional electrical stimulation (FES) and Neuroprostheses. This would require the recording of neural activity from the nerve site using special electrodes, conditioning of the signal using filters, interpreting and translating the result into an appropriate stimulus (through a circuit or algorithm). The stimulus is fed either to the terminal motor nerves in FES systems, or to control a prosthetic.

Signals and Electrodes

In this experiment, a transversely implanted multichannel silicon electrode array is used for recording the action potentials, it is an intrafascicular type electrode and belongs to a class of intraneural penetrating electrodes [5]. Compared to widely used extraneural cuff electrodes which can only record compound action potentials (CAPs) due to its physical placement around the nerve, intrafascicular electrodes penetrate into the fascicles of the nerve allowing their active sites to be located in the space between axons, thus they are able to measure the activity from a single axon unit [5] [6]. When recording, a higher S/N ratio is achieved compared to extraneural electrodes [5]. The drawbacks however are its recording stability, biocompatibility and robustness [5], so it can cause nerve damage during the insertion process [6]. It should be noted that electrodes of this nature tend to have high impedances (up to 3 MΩ) depending on the size of the recording sites [7] . The bandwidth of the action potentials measured using intrafascicular type electrodes range from 1-10 kHz. Fig 1.1 shows the bandwidth of the nerve signals measured using longitudinal intrafascicular electrodes (LIFEs) [8]. The magnitude of the nerve signals measured using intrafascicular electrodes is in the range of 200-350 µVpp [9].

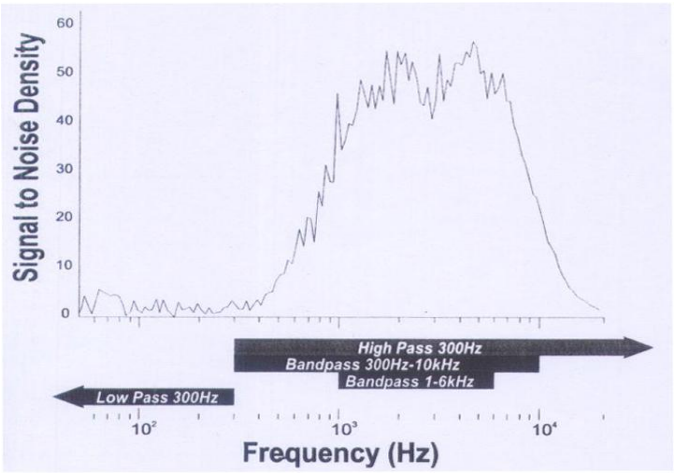


Fig 1.1
Bandwidth of the neural signal represented by the signal to noise spectrum of the LIFE recording [8]

1.2 OBJECTIVES

The project's focus is on designing and implementing a 64-channel peripheral nerve recording system using discrete components. The recorder has been designed to work with the existing Data Acquisition System (DAQ) and software with only slight modifications. Fig 1.2 shows how the nerve recorder interfaces with the DAQ.

Essentially, the data acquisition unit (DAQ) requests 1 of 64 channels through a 6-bit address supplied to the recorder, the recorder responds by supplying the DAQ with the correct filtered, differenced and amplified signal. The software running behind the DAQ is then able to separate the single stream of data back into their respective 64 channels; this can then be displayed or interpreted. The maximum data acquisition rate of current Data Acquisition Unit is 1 channel change/µs. The proposed system is designed to be compatible or faster than this rate.

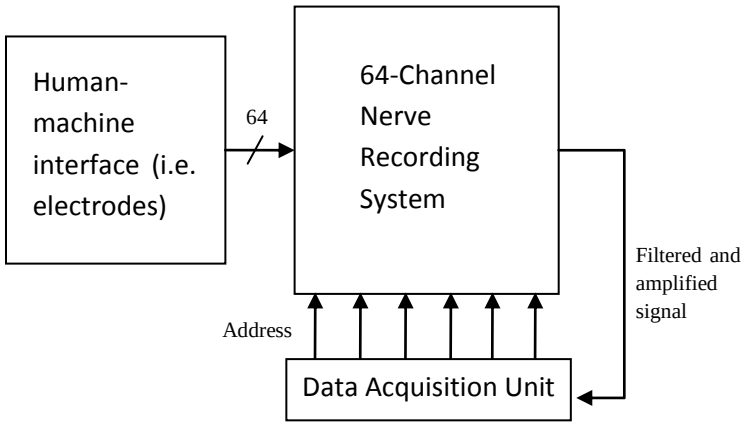


Fig 1.2
Functionality of the 64-Channel Nerve Recording System

1.3 CURRENT WORK

The final aim is to achieve a bionic neural link capable of bypassing damaged nerves to stimulate muscles directly. Fig 1.3 shows the different subsystems involved. Currently, work has been done by different teams working on the electrodes, recording, stimulation and wireless power portions of the system. Presently, the interpretation subsystem has been done in Labview, its job is to decode a continuous stream of ADC data into its respective channels and display them on a monitor.

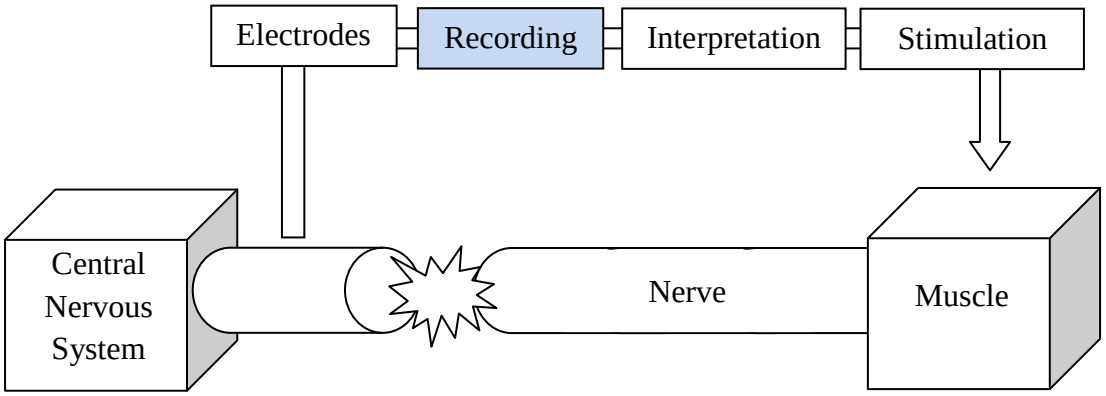


Fig 1.3
Subsystems of a Bionic Neural Link

1.4 Organization of Report

Chapter 1 gives a brief overview of the relevant concepts and motivations behind the project. Also, the objectives and scope of the project with respect to the other subsystems and work being done is presented.

Chapter 2 summarizes the system specifications for easy reference.

Chapter 3 forms the bulk of the report and details the design process. It includes important calculations such as noise and, design specifications, choice of components and certain design issues.

Chapter 4 describes how the final system has been implemented physically. This includes the PCB, power module, level shifter and other hardware.

Chapter 5 presents the all the experimental results that were obtained from the final physical system. It also includes the validation between results and design specifications.

Finally Chapter 6 ends with the concluding remarks, possible extensions and applications of the project and also possible future work.

CHAPTER 2

SYSTEM SPECIFICATIONS

The final system specifications are presented in this chapter as an easy reference. Table 2.1 shows the final system specifications and Fig 5.2 shows the frequency response of a single channel.

Table 2.1
System Specifications

Gain	59.25dB at 3kHz
Bandwidth (-3dB)	1kHz to 10kHz
Noise (RTI)	2μVrms
CMRR (at 50Hz)	37.4dB
Maximum sampling rate per channel	31250 Hz
Power consumption	1.356W
Estimated life using a 9V battery	3.33 hours

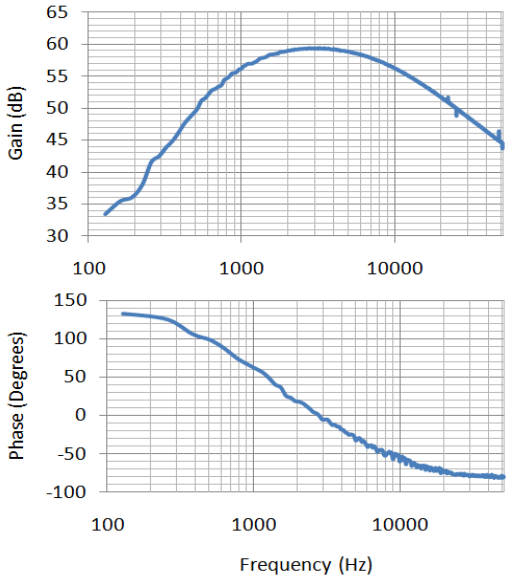


Fig 5.2
Bode Plot obtained from a spectrum analyzer on a single channel

CHAPTER 3

SYSTEM DESIGN

Chapter 3 deals with the design and simulation of the 64 channel nerve recorder. The full system model is presented in section 3.1 and is followed by a brief overview of the functions of the different stages. More detailed explanations and analyses of each stage are given in the subsequent sections namely 3.2, 3.3 and 3.4. Decisions made in certain areas of design are reasoned in the sections “Choice of Components” and “Design Issues”. Finally, a full system simulation is carried out in section 3.5 as a verification of the design.

Simulations were done in TINA SPICE. Analysis and calculations were made while consulting with the respective component’s datasheet.

3.1 SYSTEM BLOCK DIAGRAM AND OVERVIEW

The full system model as shown in Fig 3.1 is proposed.

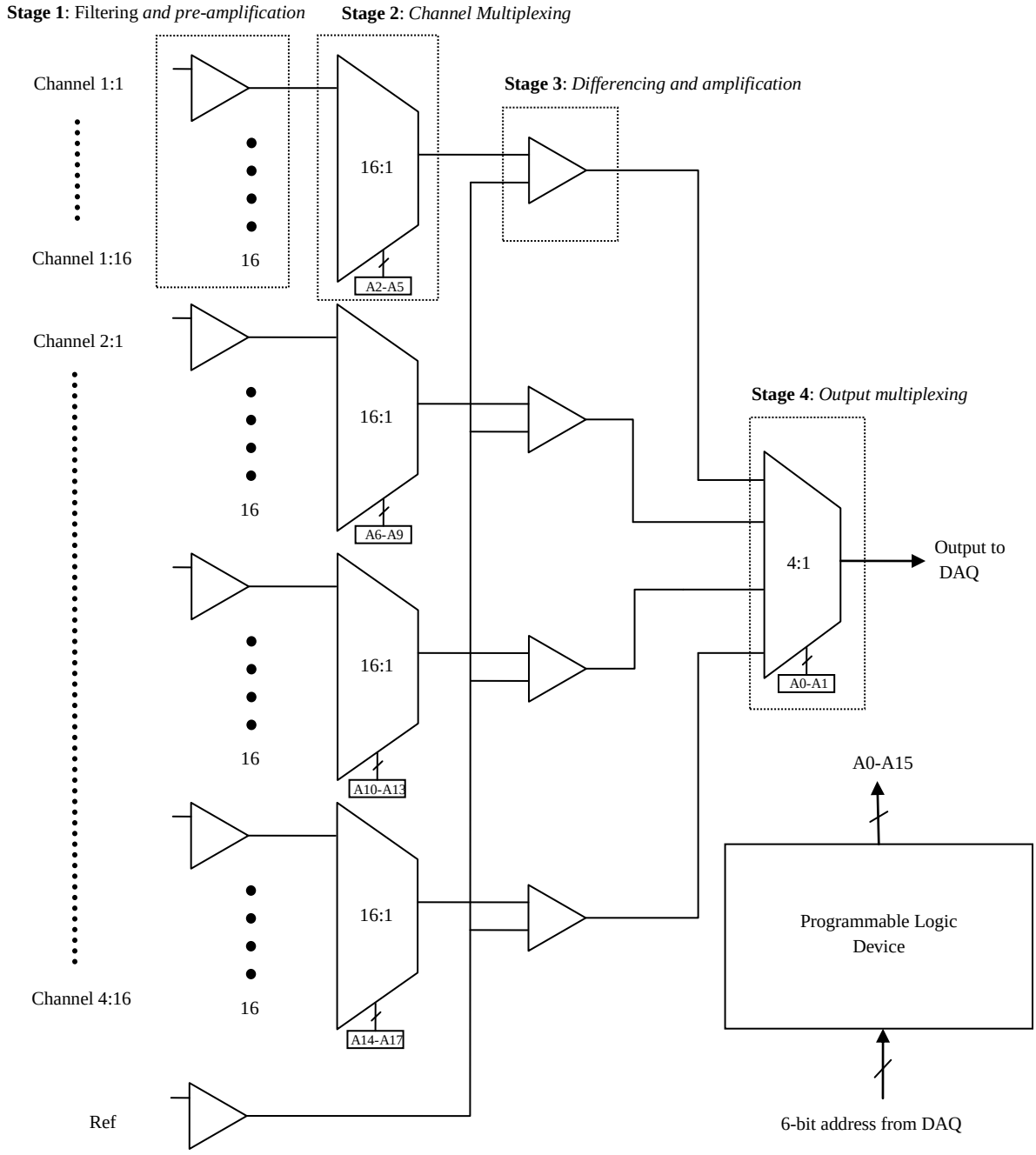


Fig 3.1
Block diagram of the full system model

Stage 1: Filtering and pre-amplification

This is the stage that is in immediate contact with the raw electrode signal. Here, the signals are filtered, pre-amplified and then fed into a 16:1 multiplexer. It should be noted that all filtering is done in stage 1.

Stage 2: Channel Multiplexing

This stage multiplexes 1 of 16 front end amplifiers to be differenced with a reference channel. The 4-bit multiplexer address comes from the Programmable Logic Device which first processes the actual channel address given by the Data Acquisition Unit.

Stage 3: Differencing and Amplification

Stage 3 consists of a differencing amplifier; the purpose of this stage is to mainly remove 50Hz line noise and any movement or physiological artifacts. No filtering is done in this stage other than the amplifier's own bandwidth. It should be noted this difference amplifier is being multiplexed into, thus the step response characteristics are of interest.

Stage 4: Output Multiplexing

This stage multiplexes 1 of 4 of the outputs from stage 3 to the Data Acquisition unit. The 2-bit multiplexer address comes from the Programmable Logic Device which first processes the actual channel address given by the Data Acquisition Unit.

Programmable Logic Device

This component interfaces the Data Acquisition Unit to the recorder and makes the recorder compatible with the current software. The Programmable Logic Device decodes the 6-bit (64) address from the Data Acquisition Unit into four 4-bit addresses for each stage 2 multiplexer and one 2-bit address for the stage 4 multiplexer.

A preemptive algorithm is used to allow for more time for the signals in stage 3 to settle before stage 4 multiplexes it to the Data Acquisition Unit thus increasing the maximum data acquisition rate. More on this is discussed in a later section.

3.2 Design and Simulation: Analog Chain

The analog chain shown in Fig 3.2 includes both stages 1 and 3. The design specifications and calculated values are summarized in Table 3.1.

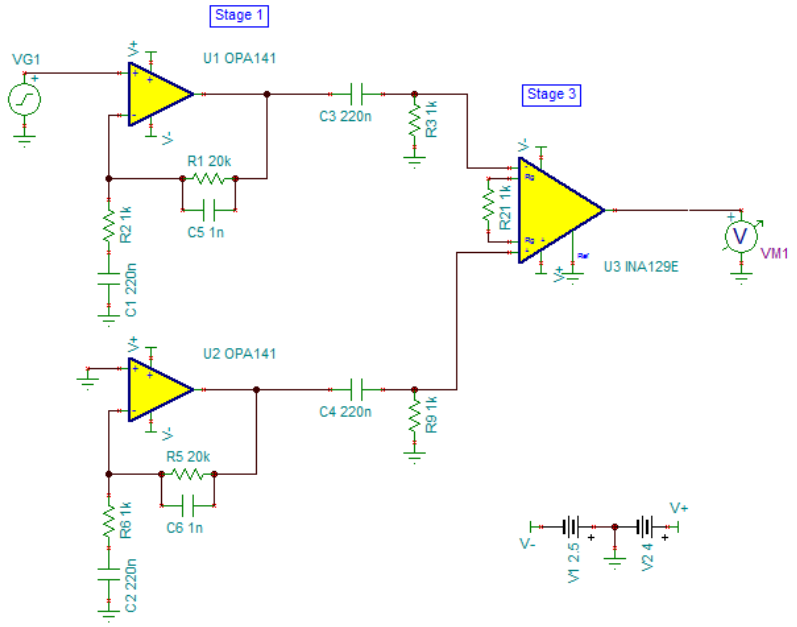


Fig 3.2
SPICE schematic of analog stages 1 and 3

Table 3.1
Design specifications of the analog chain

Design Specifications	
Frequency Response (-3dB)	1 - 8.5 kHz
Gain at mid-band	1000 at 3 kHz
Gain at 50Hz	5.6 at 50 Hz
Noise (RTI)	1µVrms
Settling time, 0.01% (Stage 3)	~8µs at 50 V/V

3.2.1 Frequency and Phase Response

A single low pass pole at 8 kHz was calculated to be sufficient in meeting the noise requirement while capturing most of the nerve signal's frequency band (See Fig 1.1).

A double high pass pole at 720 Hz was chosen to provide aggressive attenuation of 50 Hz line noise while not significantly reducing the nerve signal's frequency band. The amount of 50 Hz line attenuation was determined after a previous experiment showed large amounts of line noise due to the difficulty in obtaining a good electrode contact with the nerve and also due to the large electrode impedance.

Fig 3.3 shows the simulated Bode plot of the analog chain with a pass-band of 1-8.5 kHz, a gain of 1000 at 3 kHz and a gain of 5.6 at 50 Hz. The system is stable over all frequencies.

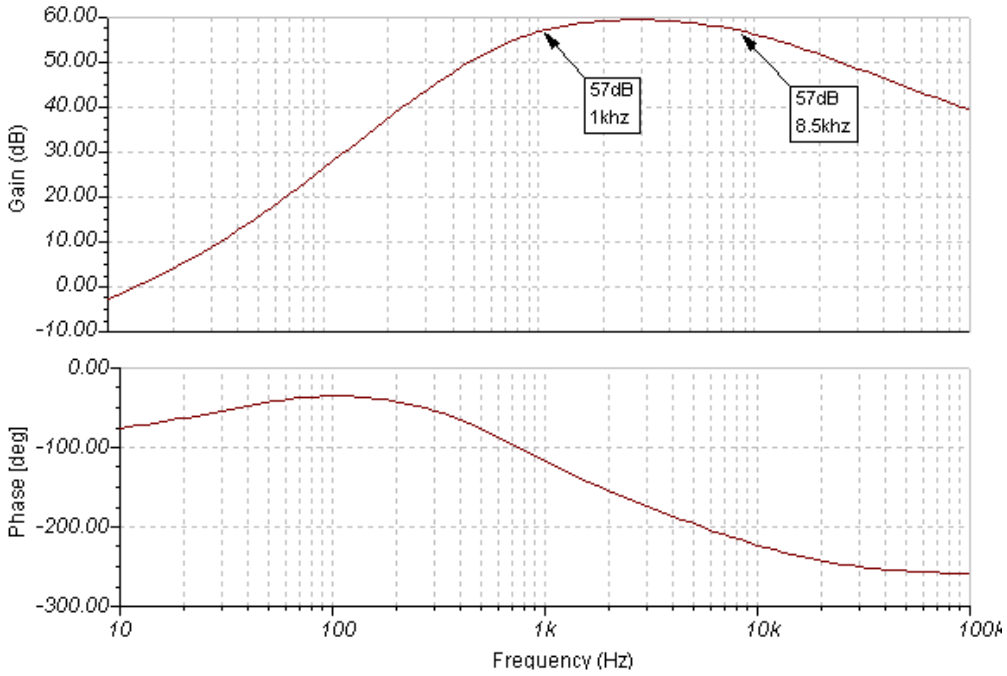


Fig 3.3
Simulated Bode Plot of the Analog Chain

3.2.2 Noise Analysis

Noise Equivalent Bandwidth for a 1st order system filtered from 720 Hz-8 kHz:

$$7280 \times 1.57 = 11.4\ kHz$$

Voltage Noise RTI due to OPA141:

$$E_{opa140,V} = 6.5n \times \sqrt{11.4k} = 0.69\mu V$$

Voltage Noise RTI due to OPA141's current noise (assume source impedance of 3MΩ):

$$E_{opa140,I} = 0.8f \times 3M \times \sqrt{11.4k} = 0.26\mu V$$

Voltage Noise RTI due to R1 (20kΩ):

$$E_{R1} = \frac{\sqrt{4kTR1}}{gain} \times \sqrt{11.4k} = \frac{\sqrt{4kT(20k)}}{21} \times \sqrt{11.4k} = 93nV$$

Voltage Noise RTI due to R2 (1kΩ):

$$E_{R2} = \frac{\sqrt{4kTR2}}{gain} \times \frac{R1}{R2} \times \sqrt{11.4k} = \frac{\sqrt{4kT \times 1k}}{21} \times \frac{20k}{1k} \times \sqrt{11.4k} = 0.41\mu V$$

Voltage Noise RTI due to R3:

$$E_{R3} = \frac{\sqrt{4kTR3}}{gain} \times \sqrt{11.4k} = \frac{\sqrt{4kT \times 1k}}{21} \times \sqrt{11.4k} = 21nV$$

Voltage Noise RTI due to INA129:

$$E_{ina129.V} = \frac{100n}{21} \times \sqrt{11.4k} = 0.51\mu V$$

Voltage Noise RTI due to INA129's current noise:

$$E_{ina129,I} = 0.3p \times 1k \times \frac{1}{21} \times \sqrt{11.4k} = 1.5nV$$

Total Noise RTI:

$$E_T = \sqrt{\left(E_{opa141,V}{}^2\right) + \left(E_{opa141,I}{}^2\right) + \left(E_{R1}{}^2\right) + \left(E_{R2}{}^2\right) + \left(E_{R3}{}^2\right) + \left(E_{ina129,V}{}^2\right) + \left(E_{ina129,I}{}^2\right)}$$

$$E_T = 1\mu Vrms$$

Note: Voltage Noise RTI due to OPA141's current noise at the inverting input is not included as it is negligible for a resistance if 1kΩ.

Maximum Noise Amplitude (99.7% of the time):

$$E_{amplitude,max} = 1\mu \times 3 = 3\mu V$$

This is small enough to contribute insignificantly to the noise of the electrode itself. For example, if the electrode impedance is already 3MΩ, the noise contributed by the electrode:

$$E_{electrode} = \sqrt{4kT3M} \times \sqrt{11.4k} = 24\mu V$$

$$E_{final} = \sqrt{\left({E_T}^2\right) + \left({E_{electrode}}^2\right)} \approx E_{electrode}$$

3.2.3 CHOICE OF COMPONENTS

Stage 1

OPA4141 by Texas Instruments was chosen as the front end amplifier due to its low voltage and current noise and its availability in a quad package. A low current noise is important as the impedances of multichannel silicon electrodes can reach values up to 3MΩ [7]. Table 3.2 summarizes the important parameters of the OPA4141.

Table 3.2
OPA4141 Important Parameters

Voltage Noise (RTI)	6.5 $nV/\sqrt{Hz}$ from 1-10kHz
Current Noise (RTI)	0.8 $fA/\sqrt{Hz}$ at 1kHz
Quiescent Current	2.3mA (max per amplifier)

Stage 3

An instrumentation amplifier was chosen for stage 3 because the high input impedance buffers the filtering components at the input. The INA129 by Texas Instruments was chosen as it has the fastest settling time in its category, this is important because the amplifier is being multiplexed into when address change occur, the settling time will thus limit the maximum achievable data acquisition rate. Table 3.3 summarizes the important parameters of the INA129.

Table 3.3
INA129 Important Parameters

Voltage Noise (RTI)	$8nV/\sqrt{Hz}$ from 1-10kHz
Current Noise (RTI)	0.3 $pA/\sqrt{Hz}$ at 1kHz
Settling Time, 0.01	7 (G=10) 9 (G=100)
CMRR	120dB (min)
Quiescent Current	700μA

3.2.4 DESIGN ISSUES

This section includes the explanations and motivations behind the design of the current system. It should be said the design was chosen as a compromise and by no means is the best design.

Size, Number of Components, Ease of Soldering and Cost

These four criteria were the main concern in implementing the design. Because the system uses discrete components, and due to the large number of channels needed (64), the system could easily become too bulky or too expensive.

For example, one extreme would be to use 64 individual instrumentation amplifiers which could easily go beyond the budget and result in a large and bulky final product. Another example would the use of second order filters which result in a large number of components needed to be soldered by hand and an increase in size and cost.

The solution was to use the same concept as the instrumentation amplifier, but to split up the gain stage and the differencing stage by adding multiplexers in between. This way, quad op-amps (OPA4141) could be used for the gain stage thus saving space. This also reduces the total number of expensive instrumentation amplifiers needed from sixty four to only four (INA129). Not to mention, the total number of components is also reduced, thus making soldering by hand easier.

Location of Filters

Several experiments were carried out to see if the passive filters could be place in stage 3 instead of stage 1; this would greatly reduce the total number of passive components needed for filtering. The attempts proved infeasible because stage 3 was being multiplexed into. Multiplexing into a low-pass pole requires the signal to settle before recording and because of the low frequency pole (5-10kHz), the signal takes a long time to settle (>50µs), making it unsuitable for the current rate of 1 channel change/µs. Multiplexing into a high-pass pole does not work because multiplexing is a series of fast impulses that are high frequency and thus they bypass the high-pass pole anyway. Also, there is a problem with the long settling time (discharging) due to the high pass pole. Thus the only solution left is to place all filters at the front such that the processed signal is always settled and never multiplexed into any poles or zeros. This will increase the number of passive components but is inevitable.

Distribution of Gain

Ideally, a high gain low noise front end is desirable to achieve a good Signal-to-Noise ratio. However, in practical applications, a low gain is used instead. Two reasons are given. First, a low gain ensures that the signal leaving stage 1 never saturates before being subtracted (common mode rejection) at stage 3. If saturation occurs before subtraction, then vital information in the signal is lost. Secondly, lowering the gain at stage 1 significantly reduces the power requirement. Instead of having high gain stages at all 64 channels, multiplexing allows the use of 64 low gain front ends and only 4 high gain amplifiers.

3.3 Design and Simulation: Multiplexing

3.3.1 Choice of Components

Stage 2

The ADG706 by Analog Devices was chosen as the second stage multiplexer due to its large number of channels (16:1) and low-power consumption of less than 0.01 µW. It also has a very low on resistance of 2.5Ω. The drawback however is the high input capacitance (200pF) that led to some cross-talk issues that will be discussed in the section 3.3.2. Table 3.4 summarizes the important parameters of the ADG706.

Table 3.4
ADG706 Important Parameters

Configuration	16:1
ON resistance	2.5 Ω
"ON" Switch capacitance	200pF
Switching Time	40ns
Power consumption	<0.01 µW

Stage 4

The ADG604 by Analog Devices was chosen as the fourth stage multiplexer due to its low input capacitance (18pF), this is important in the final stage as it reduces the settling time of the step response and thus the accuracy of the ADC sample (by ensuring that the signal has settled before reading). Also, this reduces the cross-talk between channel switching, thus increasing the maximum channel change rate. Table 3.5 summarizes the important parameters of the ADG604.

Table 3.5
ADG604 Important Parameters

Configuration	4:1
ON resistance	85 Ω
"ON" Switch capacitance	18pF
Switching Time	70ns
Supply current	0.001μA

3.3.2 DESIGN ISSUES

Cross-talk

Due to the high input capacitance of the stage 2 multiplexer (200pF), severe cross-talk was noticed between channel changes. The reason was that this capacitance together with the output resistance of stage 1 was forming an RC tank and thus will store charge from the previous switch and lead to cross talk.

The solution was to lower the resistance value to 1kΩ, thus reducing the discharge time to ground. The drawback is the increase in power due to the lower resistance.

3.4 Design and Simulation: Programmable Logic

3.4.1 Algorithm

As mentioned in the system overview, the purpose of the Programmable Logic Device is to decode the 6-bit (64 channel) address from the Data Acquisition Unit into the respective address for the stage 2 and 4 multiplexers.

A conventional way to carry out multiplexing would be to switch to the needed channels on a by demand basis. However, a closer look at the system shows that the stage 3 instrumentation amplifier needs at least a 1μs rise time after switching to get a decent settled reading. This will severely reduce the maximum data acquisition rate.

A more efficient approach is taken by fixing the channel change sequence such that more time is given to each stage 3 amplifier to settle before it is being multiplexed into stage 4. This increases the maximum data acquisition rate and accuracy of the readout.

The algorithm is as follows (refer to Fig 3.1):

1. On start up, channel 1:1, 2:1, 3:1 and 4:1 are selected by stage 2 and are already settled
2. Stage 4 reads channel 1:1
3. Stage 4 reads channel 2:1. Stage 2 switches channel 1:1 to 1:2
4. Stage 4 reads channel 3:1. Stage 2 switches channel 2:1 to 2:2
5. Stage 4 reads channel 4:1. Stage 2 switches channel 3:1 to 3:2
6. Stage 4 reads channel 1:2. Stage 2 switches channel 4:1 to 4:2
7. Stage 4 reads channel 2:2. Stage 2 switches channel 1:2 to 1:3

8. Stage 4 reads channel 3:2. Stage 2 switches channel 2:2 to 2:3
9. Stage 4 reads channel 4:2. Stage 2 switches channel 3:2 to 3:3
10. Stage 4 reads channel 1:3. Stage 2 switches channel 4:2 to 4:3
11. Continue

In effect, this algorithm preempts the next address and switches first so that when the actual address arrives, no switching of stage 2 into the difference amplifier is required thus extending the allowable settling time for each stage 3 amplifier to 3µs. However, the Data Acquisition Unit is required to read the channels in the correct order as shown in the algorithm. This system still allows the user to read from a single channel if he wishes to and is compatible with the current software.

Also note that this kind of design also allows the maximum sampling rate to scale with the number of channels required. For example, if 128 channels were required, then 8 stage 2 multiplexers would be used, this would then extend the allowable settling time to 7µs, thus allowing for a higher sampling rate.

The VHDL code for the CPLD implementing the multiplexing algorithm is included in Appendix E

3.4.3 CHOICE OF COMPONENTS

The XC2C32A CoolRunner-II CPLD by Xilinx was chosen as the programmable logic platform due to the ease and cost in obtaining the programmer for it. A cheap USB to JTAG cable from Digilent was all that was needed to program the CPLD. Also, it has a minimal logic delay of only 3.8ns; this reduces time delay between actual address input and correct output.

A total of 18 outputs (4 for each stage 2 multiplexer and 2 for the stage 4 multiplexer) and 6 inputs (6-bit address from DAQ) were required, this is supported by the 33 user IOs of the CPLD. Table 3.6 summarizes the important parameters of the XC2C32A.

Table 3.6
XC2C32A Important Parameters

Number of I/Os	33
Pin-to-pin delay	3.8ns
Voltage Supply	1.8V
Supply Current	2.5mA (max)

3.5 Design and Simulation: Full System

The full circuit schematic in SPICE is shown in Fig 3.4. The multiplexers in stages 3 and 4 are simulated by timed switches SW1-6. Only two stage 2 multiplexers are used for this simulation. The timing diagram shown in Fig 3.5 emulates the Programmable Logic Device algorithm. It should be noted that the "on" resistances and input capacitances of the multiplexers are not included in this simulation as the goal was to validate the switching algorithm. Fig 3.6 shows the output at stage 4.

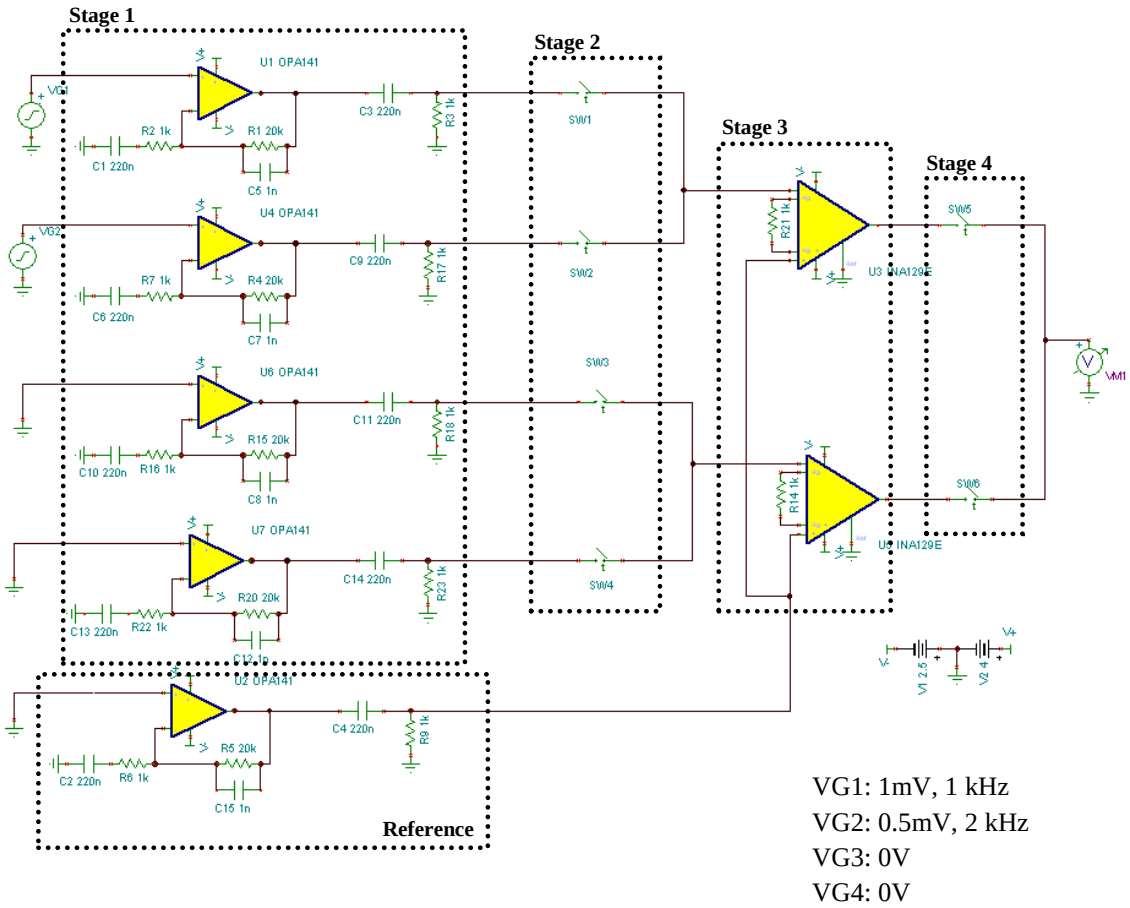


Fig 3.4
Full system SPICE schematic

0-1µs	1-2µs	2-3µs	3-4µs	4-5µs	5-6µs	6-7µs	7-8µs	8-9µs	9-10µs
SW1									
	SW5								
	SW3								
		SW6							
		SW2							
			SW5						
			SW4						
				SW6					
				SW1					
					SW5				
					SW3				

Fig 3.5

Timing diagram for switches used to emulate switching algorithm

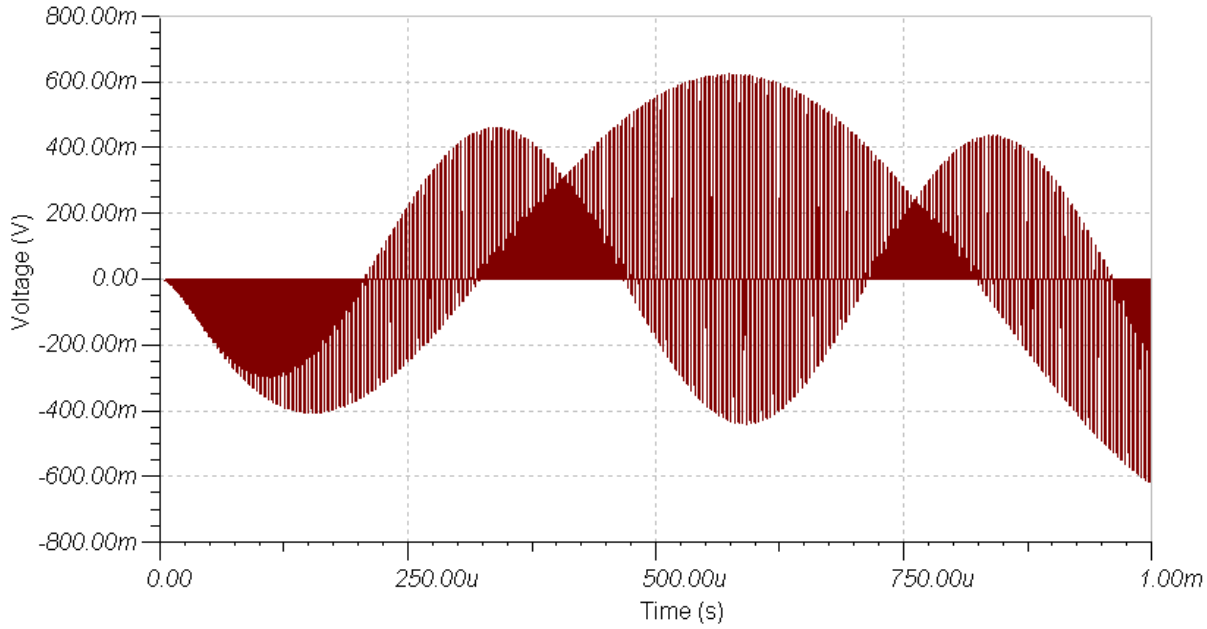


Fig 3.6

Simulated full system output

3.5.1 MODEL VALIDATION

To validate the efficiency of the switching algorithm, the signals at the output of stages 2 and 3 are shown together with the output of stage 4 in Fig 3.7. It can be seen that after stage 3 switches, a 1µs allowance is given for the output of stage 3 to settle before stage 4 switches to read the signal. It can be seen from Fig 3.7 that the INA129 at stage 3 requires at least a 1.5µs allowance before an acceptable reading should be taken. In this case, because the reading was taken only 1µs after channel 2 switches, an inaccurate reading was taken. In the actual system, four stage 2 multiplexers would be used thus giving an allowance of 3µs, more than enough for the output of stage 3 to settle.

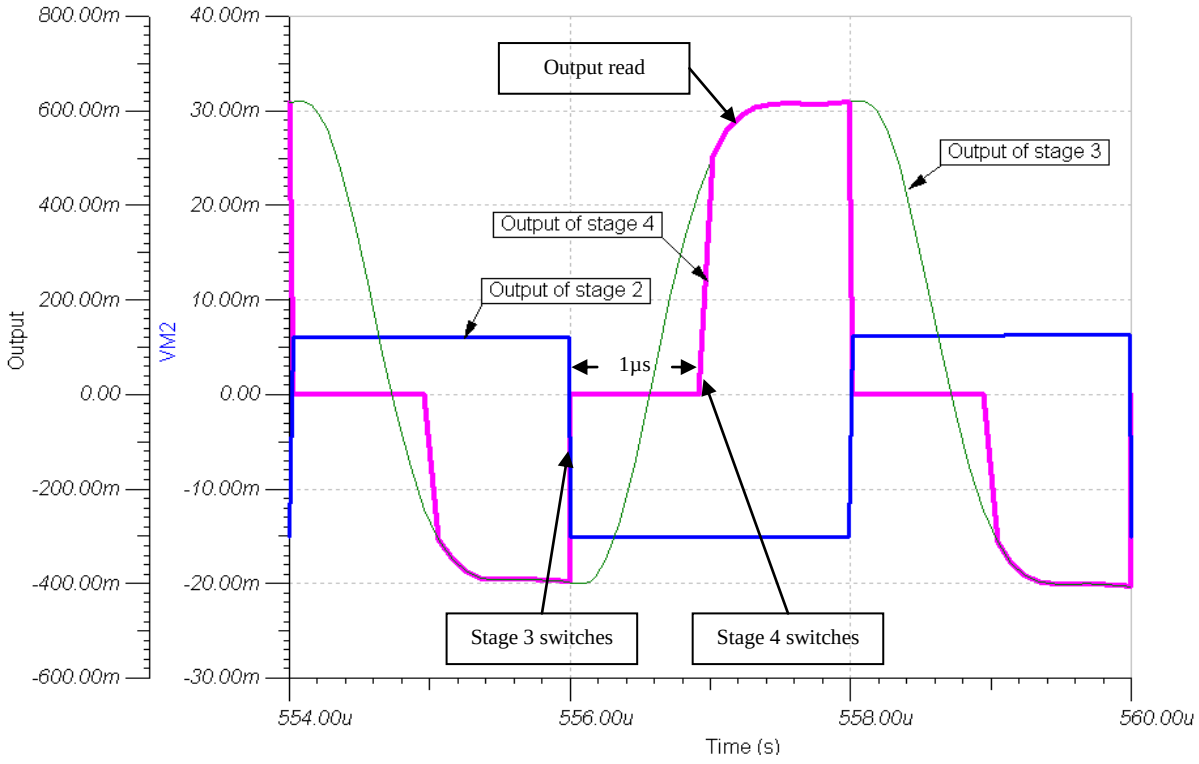


Fig 3.7
SPICE simulation analyzing the output at different stages

CHAPTER 4

PHYSICAL IMPLEMENTATION

4.1 PCB DESIGN AND IMPLEMENTATION

Fig 4.1 and 4.2 show the main board which is fully functional with 16 input channels (15 channels and 1 reference). Three expansion boards which consist of an additional stage 1, stage 2 and stage 3 would be stacked above the main board to expand the number of channels to 64. Fig 4.3 shows one of the expansion boards. The PCB design of the main and expansion board is included in Appendix A and Appendix B respectively.

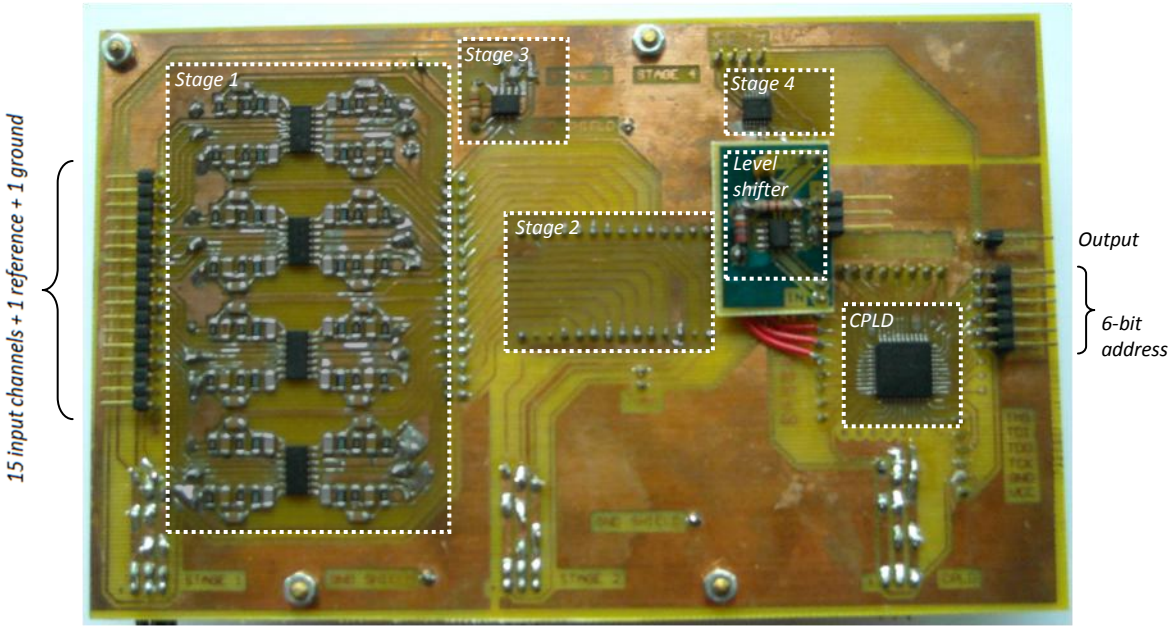


Fig 4.1
Front of the main board

Note that the stage 2 multiplexer is located behind the board and is sandwiched between two ground planes.

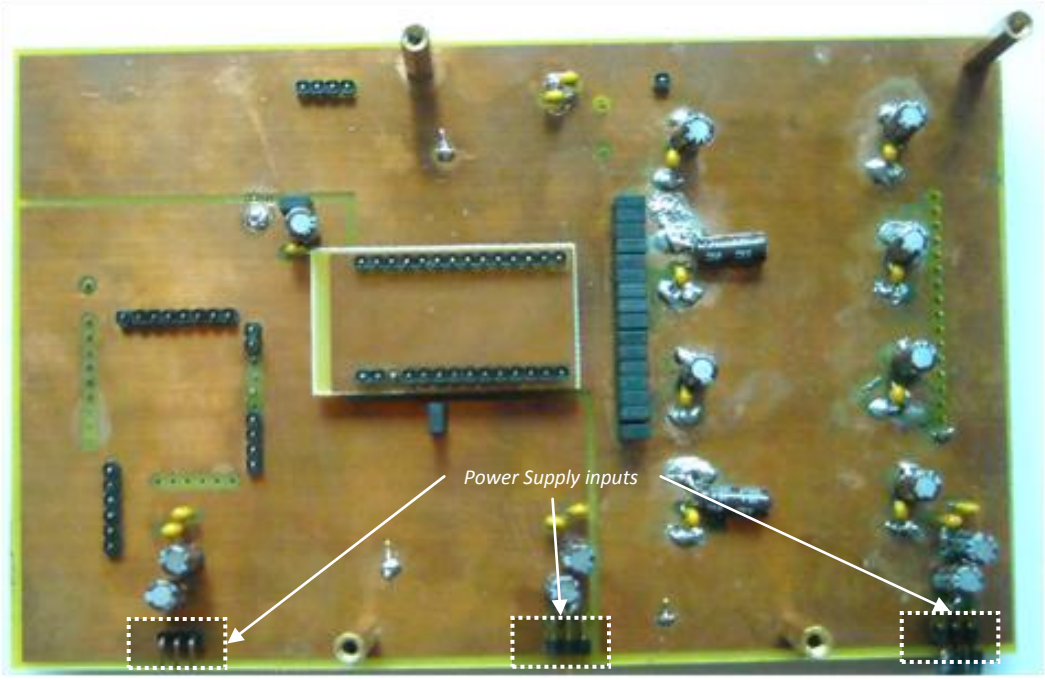


Fig 4.2
Back of the main board

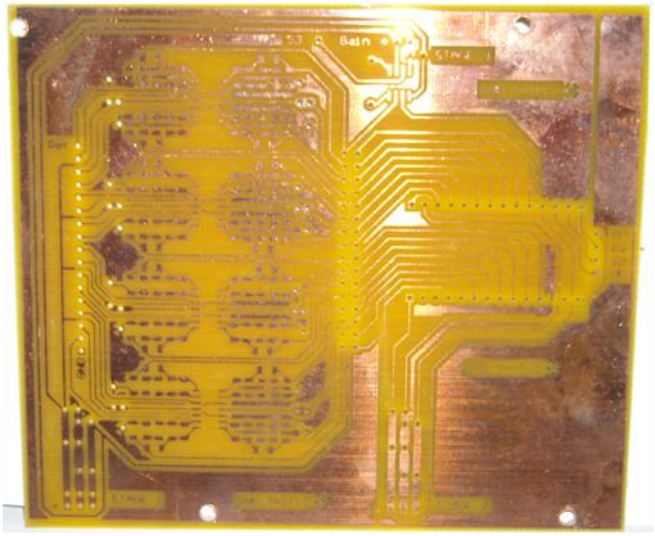


Fig 4.3
Expansion board

4.1.1 IMPLEMENTATION ISSUES

Decoupling Capacitors

Decoupling capacitors (1µF and 100µF) are placed on the back of the main board for all the power lines and also front end amplifiers as shown in Fig 4.2. This reduces the noise from the switching power supply and the noise being coupled from the digital to analog stages.

Grounding

Apart from decoupling the supplies and front end analog amplifiers, the grounding is separated into analog and digital ground as shown in Fig 4.4. Amplifiers and multiplexers are considered as analog components while the CPLD and level shifter are considered digital components. Digital components add switching noise into the power lines and ground, separating the grounds minimizes this noise being coupled into the analog stages, especially the more sensitive front end amplifiers.

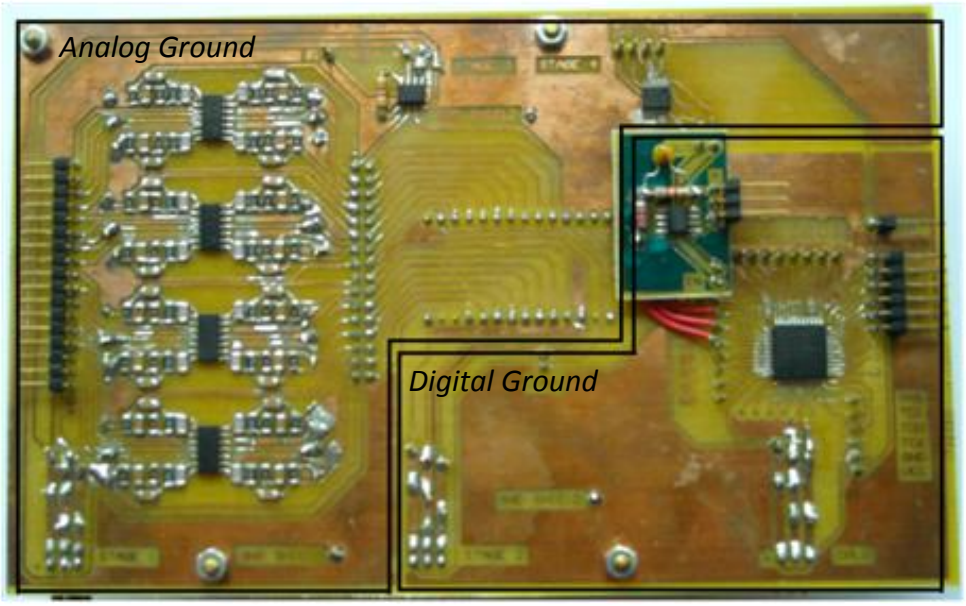


Fig 4.4
Analog and Digital grounds

4.2 LEVEL SHIFTING

The level shifter shown in Fig 4.1 was added during the debug phase when it was found that incorrect address voltage levels (0V and 1.8V) were supplied to the stage 4 multiplexer. A correction was made by adding a high speed comparator to get the correct voltage levels (-2.5V and 1.8V). This was done by biasing the inverting input of the comparator at 0.9V using a resistor network while feeding the signal to the non inverting input. The supply of the comparator was set at -2.5V and 1.8V

TLV3502AIDG4 which is a high speed comparator from Texas Instruments was chosen due to its quick response time of 4.5ns. Table 4.1 shows the important parameters of the TLV3502AIDG4.

Table 4.1
TLV3502AIDG4 Important Parameters

Supply Voltage	+2.7V to +5.5V
Supply Current	3.2mA
Response time	4.5ns

4.3 POWER MODULE

The power supply module was made on a separate PCB as shown in Fig 4.5. The module is powered by a single 9V battery and generates all the required voltages for the different stages. To save on the number of DC-DC converters needed, only three different voltages were generated (+4V, +1.8V, -2.5V), these are then distributed among the different stages according to Table 4.2.

The PCB design for the power module is included in Appendix C.

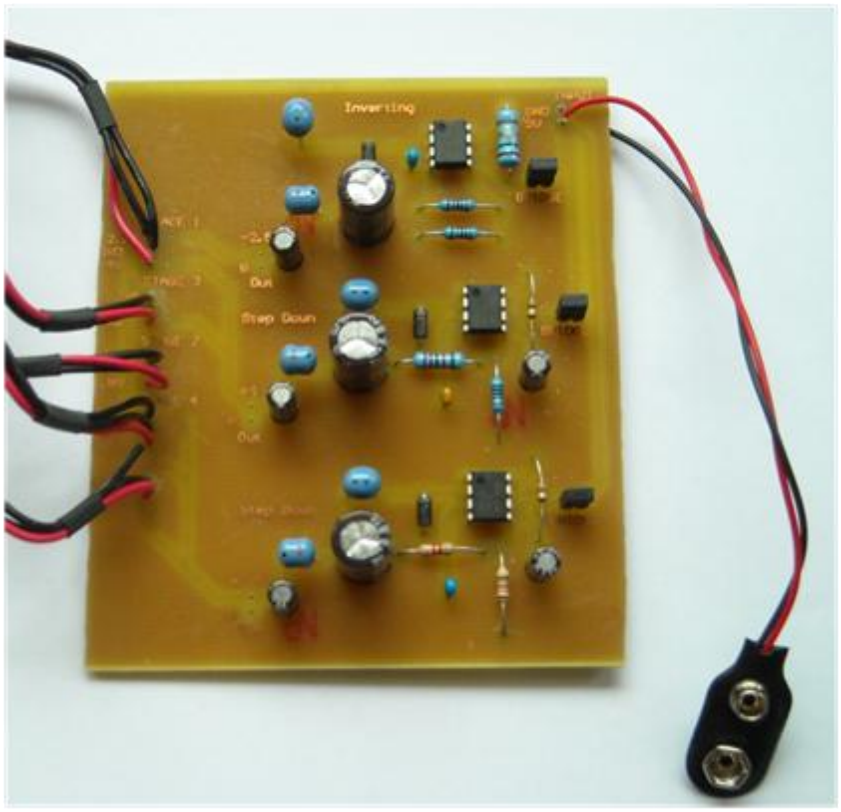


Fig 4.5
Power Module

Table 4.2
Supply voltages for respective components

Stage	Components	Component's +VE supply	Component's GND	Component's -VE supply
1 + 3	OPA4141	+4V	GND	-2.5V
	INA129	+4V	GND	-2.5V
2 + 4	ADG706	1.8V	GND	-2.5V
	ADG604	1.8V	-2.5V	N.A
CPLD	XC2C32A	1.8V	GND	N.A
Level Shifter	TLV3502AIDG4	1.8V	-2.5V	N.A

Note: Components without a negative supply are in a single supply configuration.

4.3.1 CHOICE OF COMPONENTS

The MC34063 DC-DC converter was chosen to convert the voltages. It is a switching regulator capable of operating in step-down, step-up and voltage-inverting modes, which makes it convenient to design for the different voltages needed.

Fig 4.6 and Fig 4.7 show the step-down and inverting configurations of the MC34063 respectively. An excel spreadsheet as shown in Table 4.3 - 4.5 was made to calculate the component values. The relevant equations can be found in Appendix D.

Each DC-DC converter was designed for a 100mA output current and 0.01Vpp ripple voltage. The frequency was set to the maximum of 100 kHz to minimize component values. The optional filter as shown in Fig 4.6 and 4.7 was included to further reduce the switching noise.

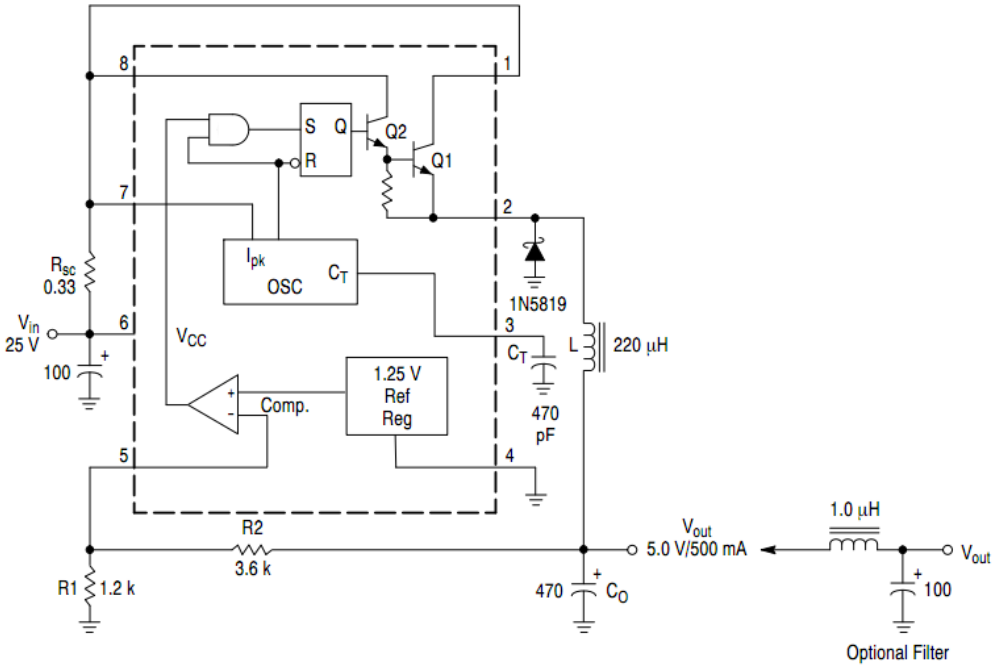


Fig 4.6
MC34063 in step-down configuration
Taken from On Semiconductor

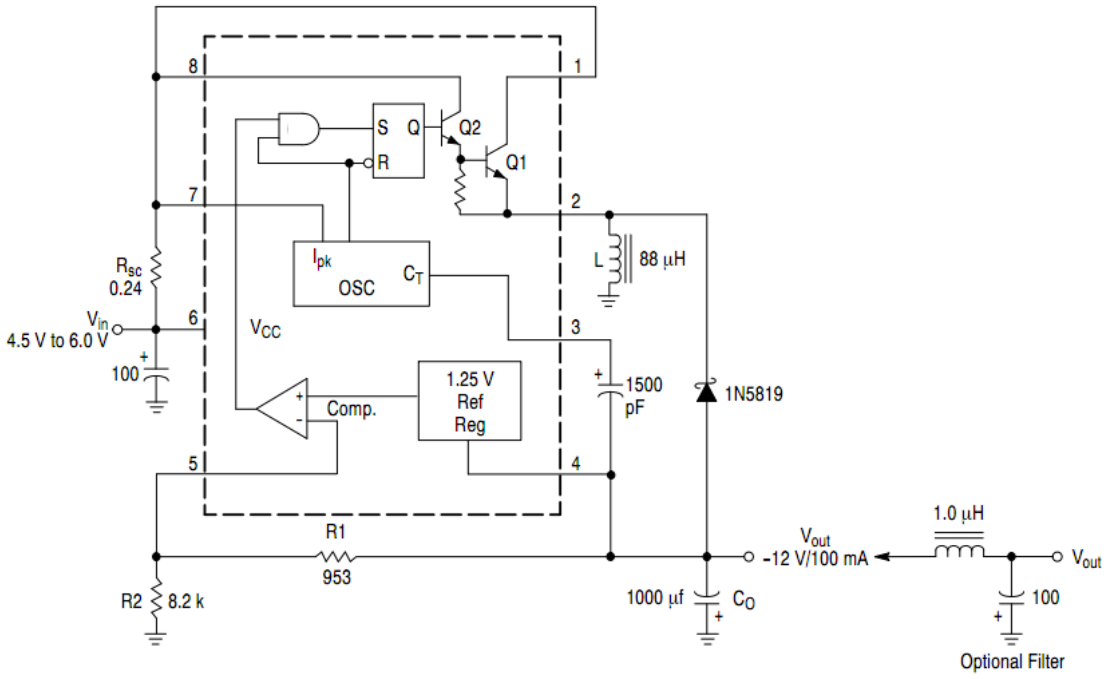


Fig 4.7
MC34063 in inverting configuration
Taken from On Semiconductor

Table 4.3
Component values for MC34063 in +1.8V step-down

Input Specifications							
$\|Vout\|$	Vf	Vin	$Vsat$	f	$Iout$	$Vripple$	$R1$
1.8	0.4	8	1	100000	0.1	0.01	10000

Component values needed	
Rsc	1.5
L	7.72973E-05
Ct	1.18919E-10
Co	0.000025
$R1$	10000
$R2$	4400

Other Components needed	
IN5819	x1
100µF	x2
1µH	x1

** Vf is the forward voltage drop of the diode IN5819*

Table 4.4

Component values for MC34063 in -2.5V inverting mode

Input Specifications							
$\|Vout\|$	Vf	Vin	$Vsat$	f	$Iout$	$Vripple$	$R1$
-2.5	0.4	8	1	100000	0.1	0.01	10000

Component values needed	
Rsc	1.060606061
L	7.24926E-05
Ct	1.17172E-10
Co	0.000263636
$R1$	10000
$R2$	10000

Other Components needed	
IN5819	x1
100µF	x2
1µH	x1

Table 4.5

Component values for MC34063 in +4V step-down

Input Specifications							
$\|Vout\|$	Vf	Vin	$Vsat$	f	$Iout$	$Vripple$	$R1$
4	0.4	8	1	100000	0.1	0.01	10000

Component values needed	
Rsc	1.5
L	8.91892E-05
Ct	2.37838E-10
Co	0.000025
$R1$	10000
$R2$	22000

Other Components needed	
IN5819	x1
100µF	x2
1µH	x1

Additional notes

The actual values of L, Ct and Co used were rounded up to the next largest component value available since those calculated are not in the standard values available.

4.4 Other Hardware

4.4.1 Aluminum Housing

An aluminum housing shown in Fig 4.8 was made to enclose the main board and power supply; this would reduce the amount of noise being picked up by the circuit boards.

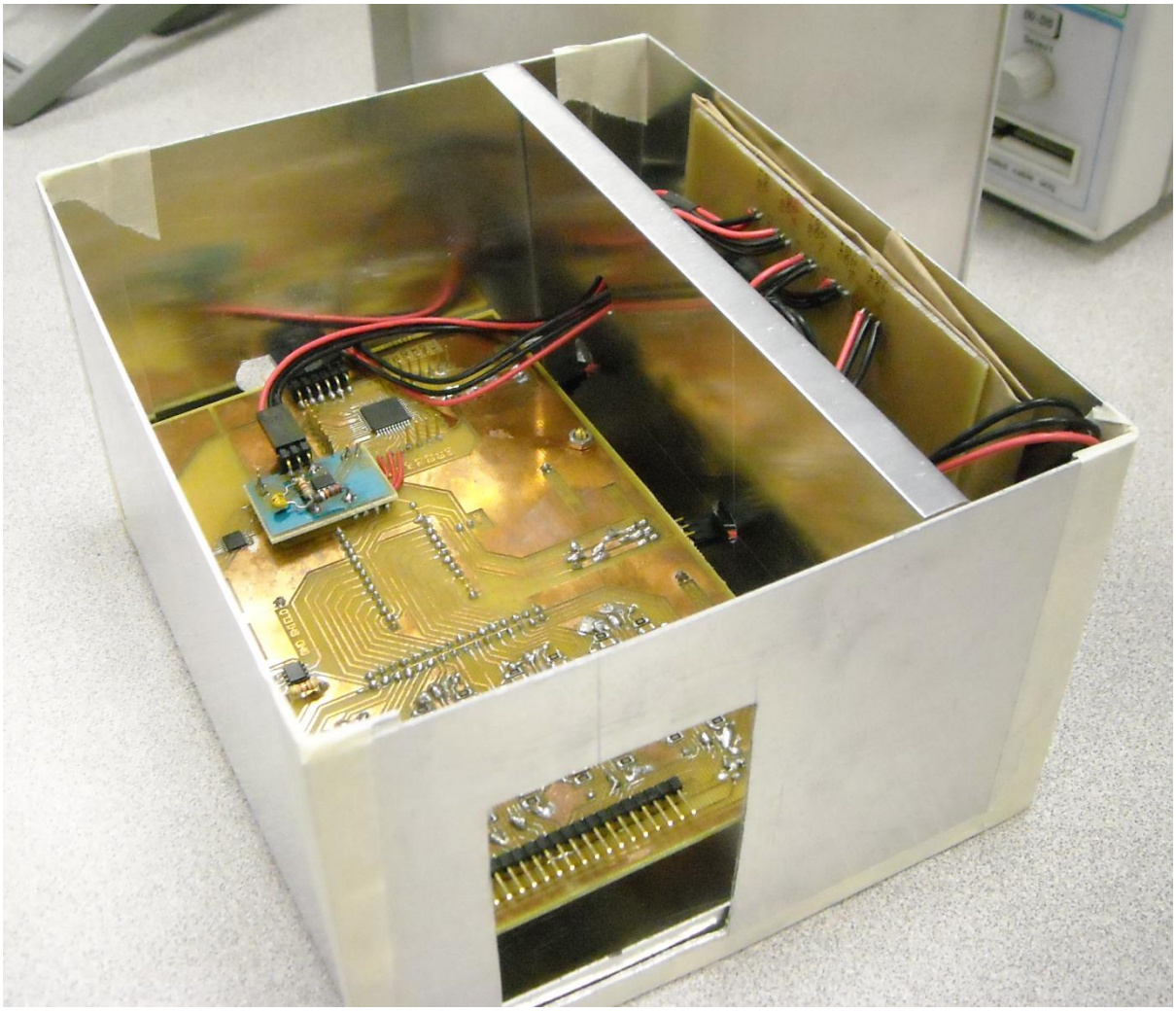


Fig 4.8
Aluminum housing for main board and power supply

4.4.2 Electrode Insertion and Stabilization

Other than the recording system, an electrode insertion setup was also constructed as shown in Fig 4.9. The full setup consists of the following

- 12 by 12 inch steel plate
- 3 axis inserter mounted on a wooden frame and two bookstands
- Cooling hoses with crocodile clips attached

In addition, to stabilize the inserter and cooling hoses, neodymium magnets were attached to the bases of the bookstands and cooling hoses.

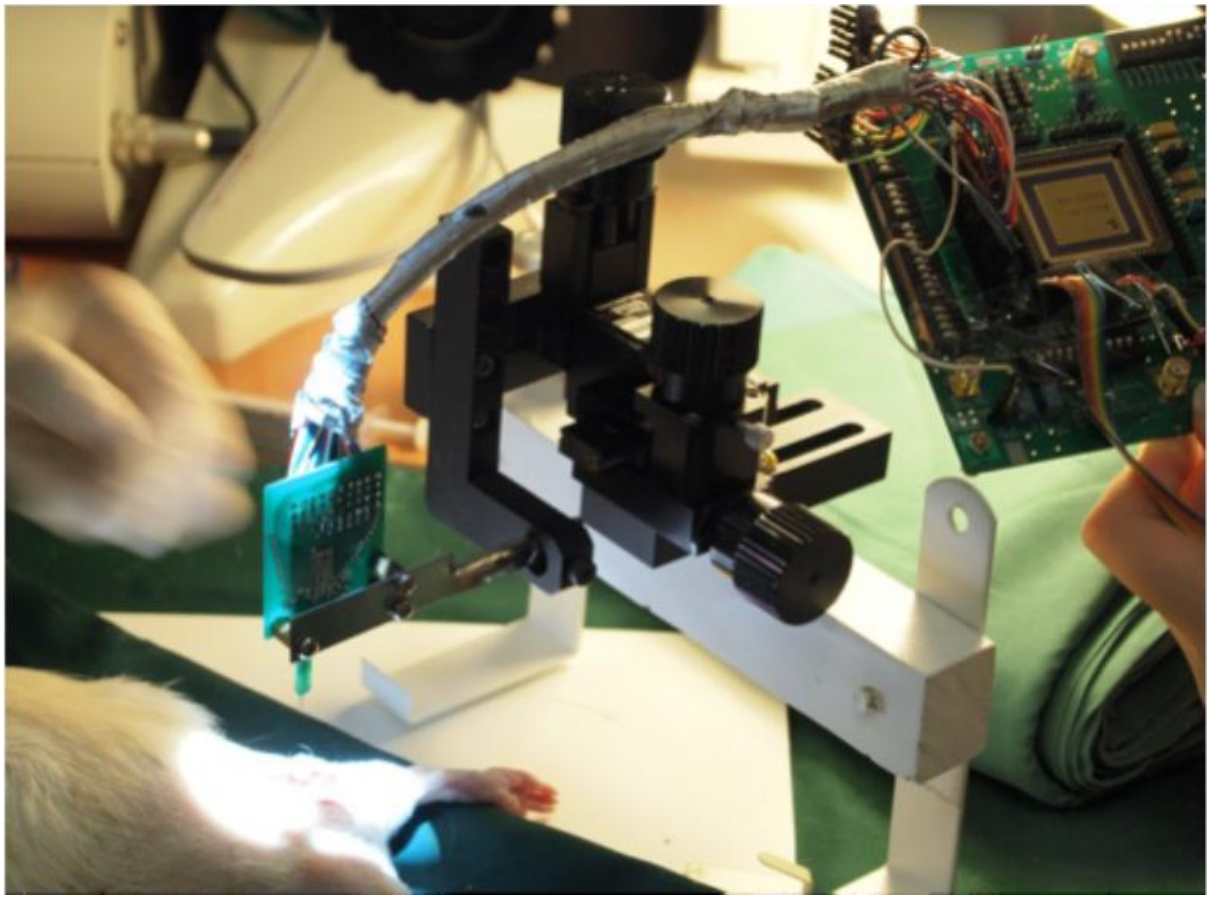


Fig 4.9
Electrode inserter and metal base

The cooling hoses provided a flexible way to manipulate the crocodile clips while being relatively stable by the attachment of neodymium magnets. Fig 4.10 shows a crocodile clip attached to a cooling hose and being used to stabilize the nerve for inserting of the electrode.

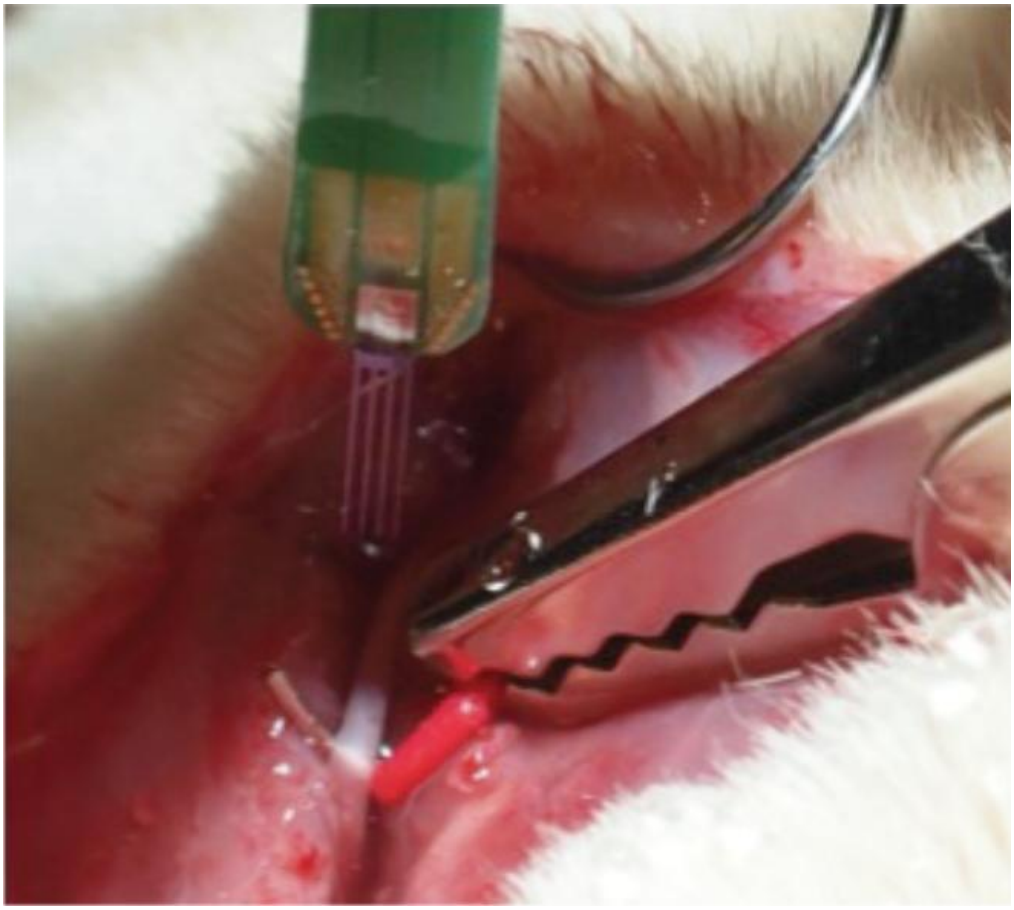


Fig 4.10
Crocodile clip attached to cooling hose (not shown in figure) stabilizing the nerve

CHAPTER 5

EXPERIMENTATION RESULTS

5.1 Experimentation Results: Analog Chain

The analog chain consists of both stages 1 and 3. The following experiments were conducted by holding a static address of one of the input channels and reading directly from the output of stage 4.

Gain

Fig 5.1 shows the output (top) to an input (bottom) of 2mVpp at 1 kHz. This gives a gain of around 750 at 1 kHz, which corresponds closely to a simulated gain of 707 at 1 kHz (see section 3.2.1).

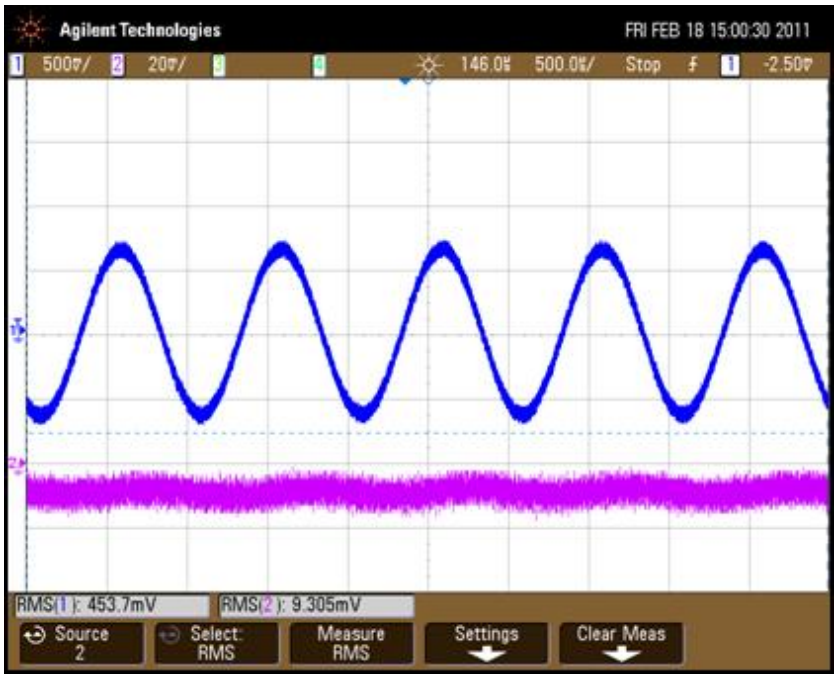


Fig 5.1
Output of a single channel to an input of a 2mVpp, 1 kHz sine wave

Frequency and Phase Response

Fig 5.2 shows a bode plot obtained from a spectrum analyzer on a single channel. Due to the limitations of the spectrum analyzer, only a maximum frequency range of 128Hz to 51200Hz is obtainable.

A peak gain of 59.25dB at 3 kHz was obtained with the -3dB bandwidth from 1 kHz to 10 kHz. The high frequency pole occurs later than the simulated 8.5 kHz (see Fig 3.3), this might be due to the large component tolerances (see Table 5.1).

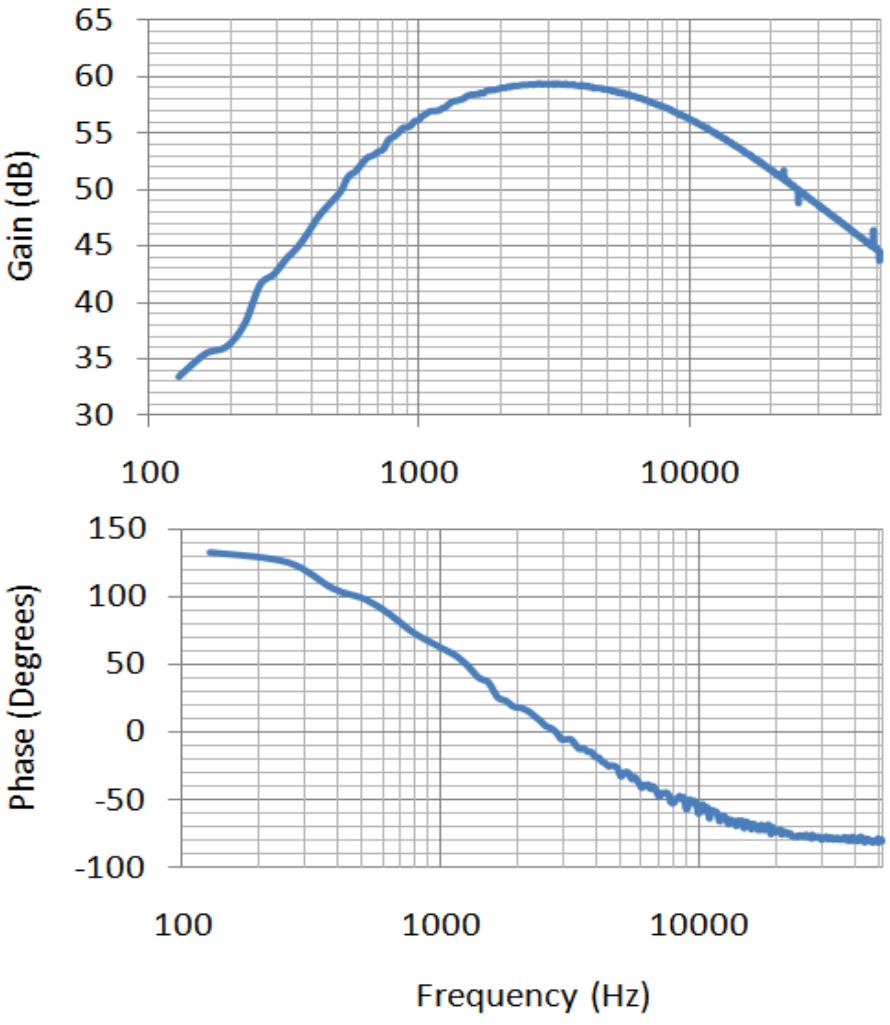


Fig 5.2
Bode Plot obtained from a spectrum analyzer on a single channel

Noise

To measure the system noise, the input channel recorded was grounded and the oscilloscope was set to be ac coupled and turned on to its highest resolution.

The leftmost graph in Fig 5.3 shows an output noise of 7.92 mVrms when the channel being recorded is grounded. The rightmost graph shows the output noise of the oscilloscope obtained by shorting the probe connectors together. An oscilloscope noise of 5.223 mVrms was measured.

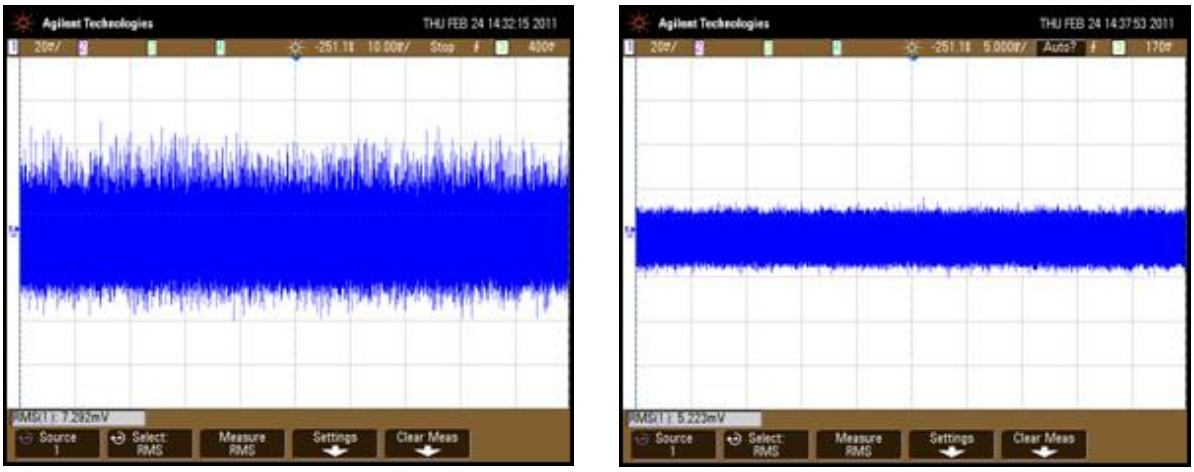
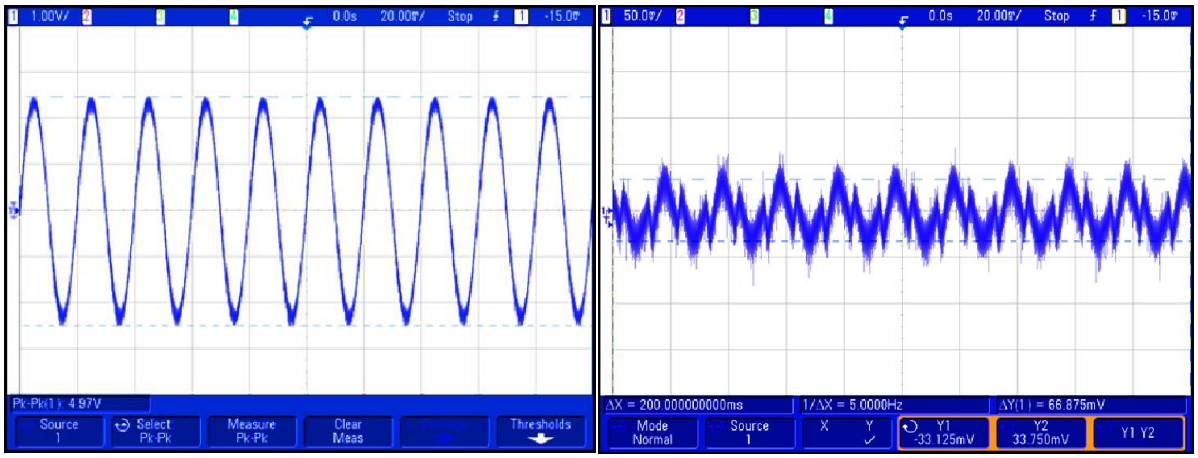


Fig 5.3
Output and oscilloscope noise of a single channel

Subtracting the output noise from the oscilloscope noise gives a true system noise of about 2 mVrms at the output. This noise occurs over a Noise Equivalent Bandwidth of 11.4 kHz (see section 3.2.2). To refer this to the input, the output noise of 2 mVrms is divided by the gain at mid band (1000 at 3 kHz); this would give a RTI noise of 2 µVrms over a Noise Equivalent Bandwidth of 11.4 kHz at the input. This is twice the simulated value (see section 3.2.2) and is to be expected since supply and any external noise sources were not considered in the calculation.

CMRR at 50Hz

To calculate the CMRR, a 700mVpp, 50 Hz, test signal was connected to one input channel and the reference was connected to ground to obtain the differential mode gain. Fig 5.4 (a) shows the output sine wave at 4.97Vpp. To obtain the common mode gain, both the reference and input were connected to the test signal. Fig 5.4 (b) shows the output in common mode with a voltage of 66.87mVpp.



(a) (b)

Fig 5.4
Output signal in differential mode (a), and common mode (b)

The CMRR at 50Hz is calculated as follows:

$$A_d = \frac{4.97}{700m} = 7.1$$

$$A_{cm} = \frac{66.87m}{700m} = 0.0955$$

$$CMRR\ at\ 50\ Hz = 20log\left(\frac{7.1}{0.0955}\right) = 37.4dB$$

The CMRR of the system is degraded due the addition of passive components in between the amplification and differencing stages as shown in Fig 3.2, as such, the reference channel and the input channel have slightly different gains. This difference is further amplified by the amplifier at stage 3, thus degrading the CMRR. Table 5.1 shows the tolerances of the passive components used. Unfortunately, this is a trade off for separating the stages to reduce the number of components needed.

To make up for the poor CMRR performance, a more aggressive low frequency cut-off was adopted.

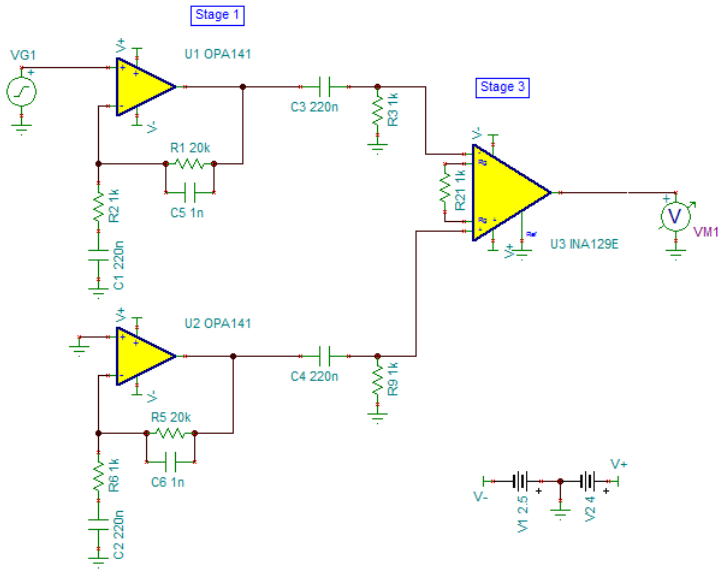


Fig 3.2
SPICE schematic of analog stages 1 and 3

Table 5.1
Component Tolerances

Component	Value	Tolerance
R1, R5	20k	1%
R2, R6,R3	1k	1%
C5, C6	1nF	5%
C1, C2,C3,C4	220nF	10%

5.2 EXPERIMENTATION RESULTS: FULL SYSTEM

Fig 5.5 shows the output signal to a 3mV amplitude 1 kHz sine wave on a single channel while the other 63 channels are being grounded. A channel change rate of 1 MHz was used. The thick noise present is actually the switching noise. Note that a 3mV amplitude signal was used to show the output on the oscilloscope clearly. The switching noise is not a problem since actual recording takes place only when the signal has settled.

Fig 5.5
Actual output at stage 4

To validate the multiplexing algorithm, three signals are shown together in Fig 5.6. Channel 3 (top) shows the input address change, channel 2 (middle) shows the output at stage 3 and channel 1 (bottom) shows the output at stage 4. The simulated version can be found in section 3.5.1.

It can be seen that when the address changes, it takes about 1 µs for the output of stage 3 to settle, this is due to the rise time incurred when stage 2 multiplexes into the INA129 in stage 3. After 3 µs from address change, stage 4 switches the output of the INA129 to the DAQ, by this time the signal is already well settled. Thus, instead of reading the output at address change, the switching algorithm gives an additional 3µs for the signal to settle. Note that an extra leeway of 2µs is left which will allow the switching frequency to go up to 2 MHz, or 31250 Hz per channel.

Fig 5.6
Model Validation

5.4 Experimentation Results: Recording Software

The multiplexed signal at the output of stage 4 is fed into the DAQ where it is de-multiplexed in software back into the respective 64 channels. To interface the dual supply recording module to the single supply DAQ, the DAQ inputs were referenced to a -2.5V source tapped from the recording module. Fig 5.7 shows the software de-multiplexed waveform graphs of 64 channels. Each graph displays up to 8 individual channels. It can be seen that the software successfully displays a 1 kHz, 2mVpp sine wave at one of the input channels. Note that 1 channel of the OPA4141 is malfunctioning and displays excessive noise, also 1 channel appears to be shorted to -2.5V in the main board, this could be due to a bad solder joint.

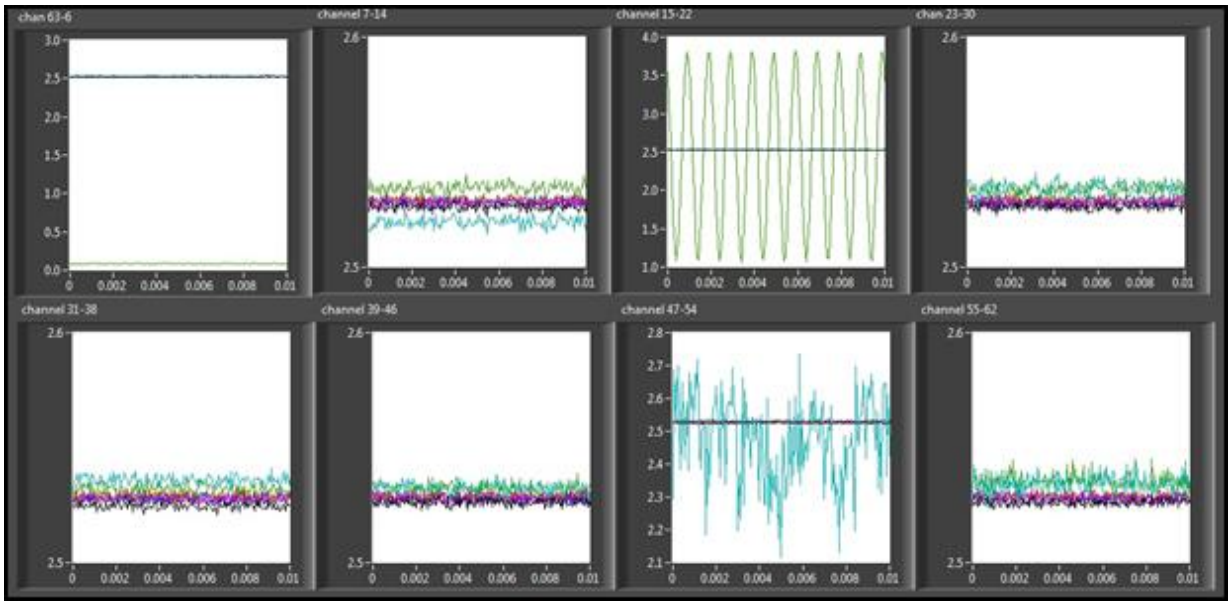


Fig 5.7
Modified recording software to support 64 channels

5.5 POWER CONSUMPTION

The total power required was calculated by multiplying the current and the voltage provided by an external power supply to the board. This measurement is taken while all the inputs are left open. Also, this calculation is only for 16 channels, as no expansion boards have yet been added.

The power drawn by the main board (see Fig 4.1):

$$Voltage\ supply = 9V$$
$$Current\ draw = 0.058A$$
$$Power\ of\ main\ board\ = 0.522W$$

To estimate the power requirement of an expansion board, the power connectors to the relevant stages were removed. The drop in power would then be the power required for an expansion board. An assumption is made that the efficiency of the power supply remains the same. In reality, the efficiency drops when the current supplied undershoots what it was designed for and since the current drawn is less than what was designed (0.1A) the calculation would be conservative.

The power drawn by the main board less expansion components:

$$Voltage\ supply = 9V$$
$$Current\ draw = 0.026A$$
$$Power = 0.234W$$

Estimated power required for an expansion board:

$$Power\ of\ expansion\ board = 0.522 - 0.234 = 0.288W$$

Estimated total power needed for the eventual system:

$$Power\ of\ fullsystem = 0.522 + 3 \times 0.288 = 1.356W$$

Fig 5.8 shows the capacity of an Energizer 522 9V battery, the battery is considered dead when the supply voltage drops to 4.8V. Since the largest voltage generated for the board is 4V in step down configuration, we assume system starts to malfunction when the supply voltage drops to 4.8V, which is reasonable.

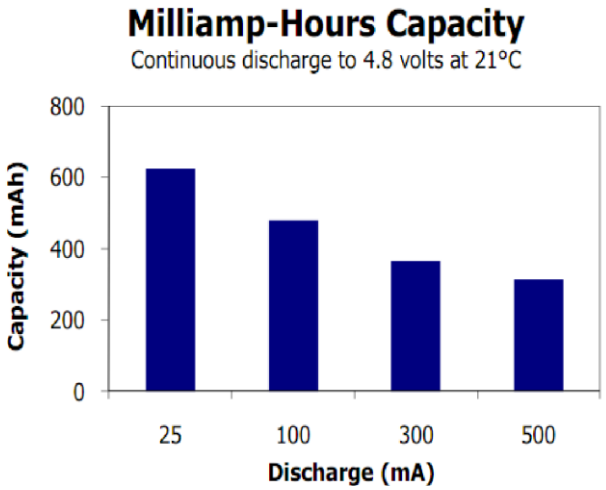


Fig 5.8
Capacity of an Energizer 522 9V battery
Taken from Energizer

The total hours of usage is calculated as follows:

$$Discharge\ current = \frac{1.356}{9} = 0.15A$$

This corresponds to about 500mAh from Fig 5.8

$$Total\ hours\ of\ usage = 500m \div 0.15 = 3.33\ hours$$

CHAPTER 6

CONCLUSION

6.1 SUMMARY OF PROBLEM AND WORK DONE

To summarize, the project's focus was to design and implement a discrete 64-channel peripheral nerve recording system which is system compatible with the current Data Acquisition Unit and recording software. The challenge was to minimize the cost and size of the board due of the large number of channels needed required. It was shown that by using a more efficient multiplexing algorithm, the size, cost and power consumption of the system can be reduced while still being able to provide a bandwidth of 30 kHz per recording channel, the drawback however was a low CMRR of 37.4 dB at 50 Hz. To make up for the poor CMRR, more aggressive low frequency attenuation was adopted.

Finally, an input referred noise of 2μVrms for each channel was achieved using a bandwidth from 1 kHz to 10 kHz with a peak gain of 59.25dB at 3 kHz. Table 2.1 shown below summarizes the final system specifications.

Other work done included the hardware setup for the animal experiments and the modification of the recording software to support 64 channels.

Table 2.1
System Specifications

Gain	59.25dB at 3kHz
Bandwidth (-3dB)	1kHz to 10kHz
Noise (RTI)	2μVrms
CMRR (at 50Hz)	37.4dB
Maximum sampling rate per channel	31250 Hz
Power consumption	1.356W
Estimated life using a 9V battery	3.33 hours

6.2 Concluding Remarks And Future Work

In conclusion, the proposed design provides an efficient way to implement a multi channel discrete system for test and measurement in a laboratory environment. However, due to its size and power consumption it is infeasible for any kind of chronic experiments.

One advantage of the proposed design is that the maximum sampling rate scales with the total number of channels needed, thus the number of channels can be increased while maintaining the same bandwidth for each channel. Another advantage of such a design is the ability to conserve power by reducing the number of high gain amplifiers.

Even though the discrete system is not suitable for implants, the same switching algorithm can be applied to integrated solutions to reduce both area and power.

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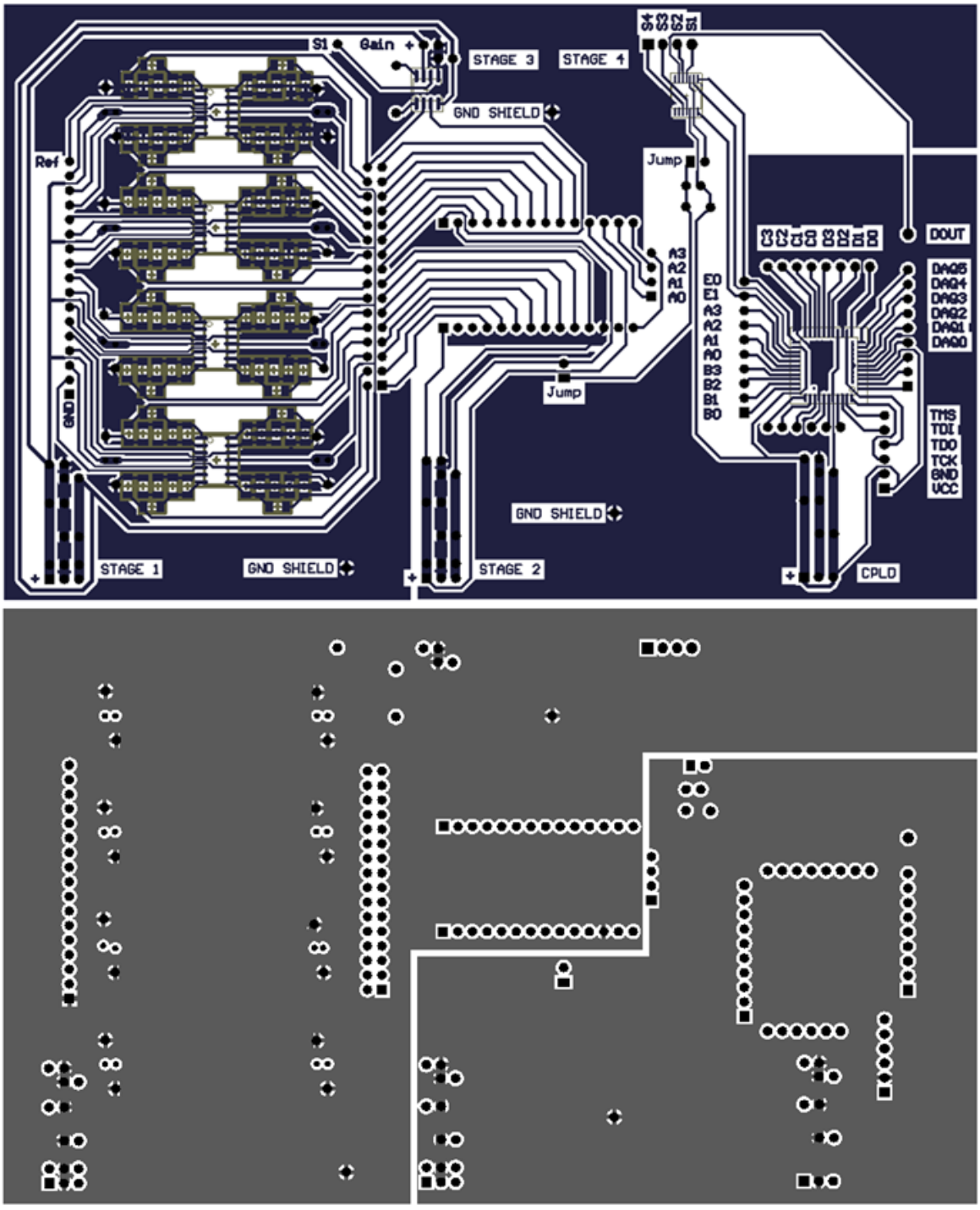
9. Jia, X., et al. *AAHS Session B3: Congenital and Nerve II*. in *American Association for Hand Surgery 2010 Annual Meeting*. 2010.

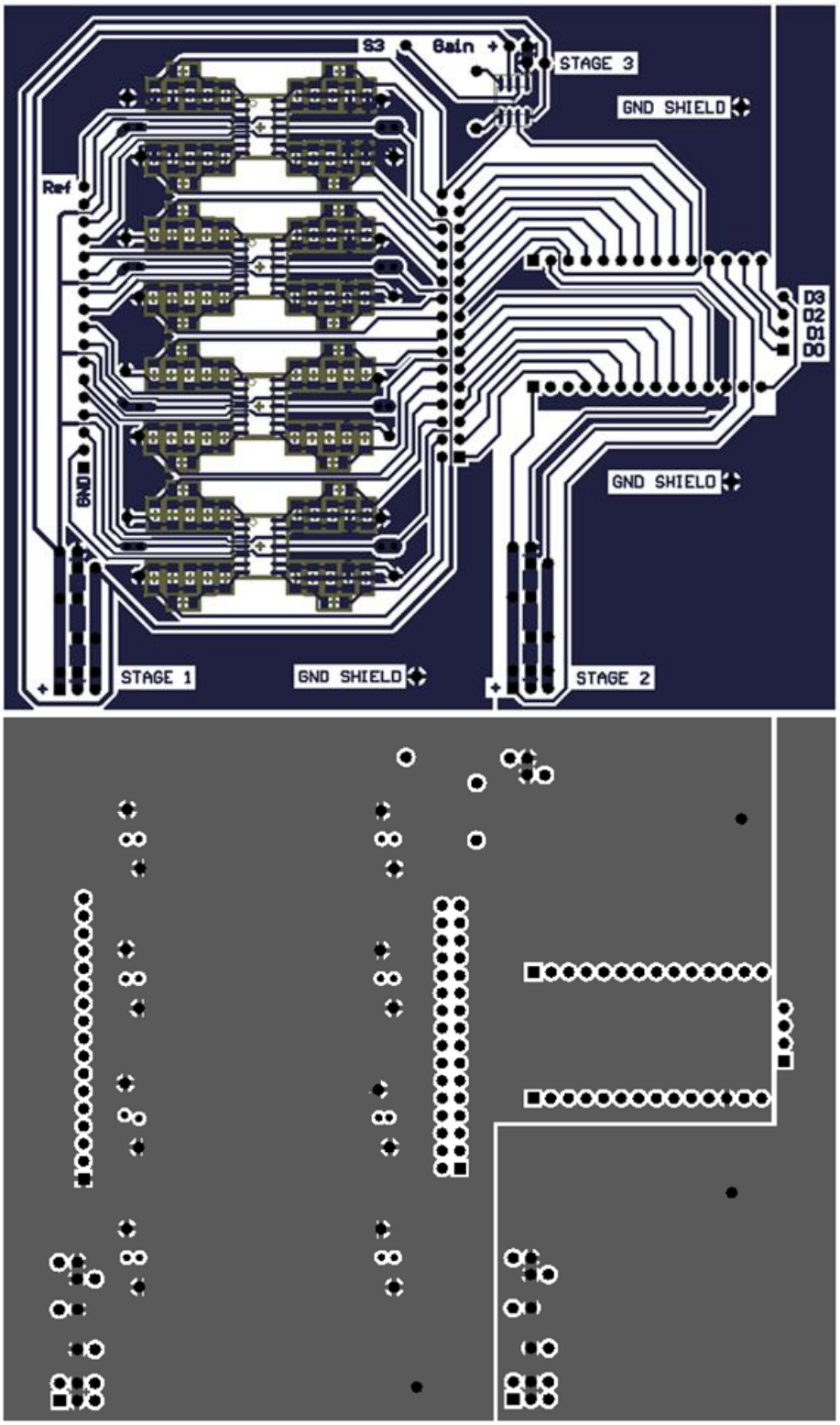
APPENDIX A

PCB of Main board



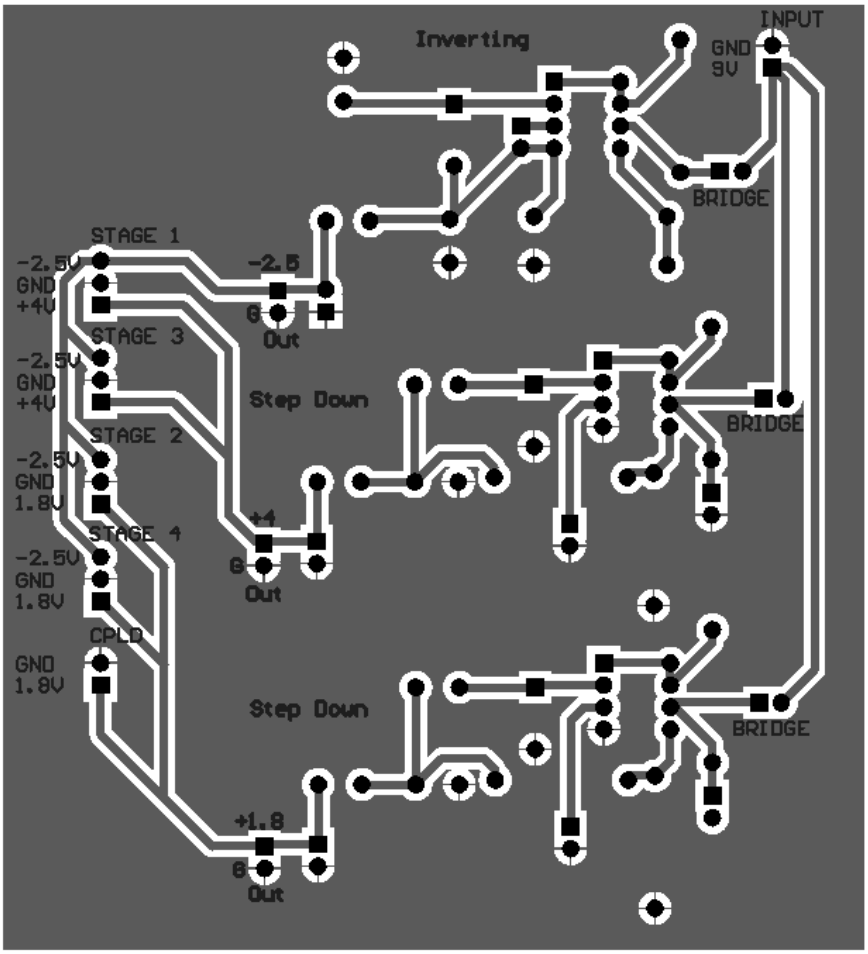
APPENDIX B

PCB of expansion board



APPENDIX C

PCB of power supply



APPENDIX D

Equations for MC34063 taken from On Semiconductor.

Calculation	Step–Up	Step–Down	Voltage–Inverting
t_{on}/t_{off}	$\frac{V_{out} + V_F - V_{in(min)}}{V_{in(min)} - V_{sat}}$	$\frac{V_{out} + V_F}{V_{in(min)} - V_{sat} - V_{out}}$	$\frac{\lvert V_{out}\rvert + V_F}{V_{in} - V_{sat}}$
$(t_{on} + t_{off})$	$\frac{1}{f}$	$\frac{1}{f}$	$\frac{1}{f}$
t_{off}	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$	$\frac{t_{on} + t_{off}}{\frac{t_{on}}{t_{off}} + 1}$
t_{on}	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$	$(t_{on} + t_{off}) - t_{off}$
C_T	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$	$4.0 \times 10^{-5}\, t_{on}$
$I_{pk(switch)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$	$2I_{out(max)}$	$2I_{out(max)}\left(\frac{t_{on}}{t_{off}} + 1\right)$
R_{sc}	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$	$0.3/I_{pk(switch)}$
$L_{(min)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat} - V_{out})}{I_{pk(switch)}}\right) t_{on(max)}$	$\left(\frac{(V_{in(min)} - V_{sat})}{I_{pk(switch)}}\right) t_{on(max)}$
C_O	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$	$\frac{I_{pk(switch)}(t_{on} + t_{off})}{8V_{ripple(pp)}}$	$9\,\frac{I_{out} t_{on}}{V_{ripple(pp)}}$

V_{sat} = Saturation voltage of the output switch.
V_F = Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{in} – Nominal input voltage.
V_{out} – Desired output voltage, $|V_{out}| = 1.25\left(1 + \frac{R2}{R1}\right)$
I_{out} – Desired output current.
f_{min} – Minimum desired output switching frequency at the selected values of V_{in} and I_O.
$V_{ripple(pp)}$ – Desired peak–to–peak output ripple voltage. In practice, the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.

NOTE: For further information refer to Application Note AN920A/D and AN954/D.

APPENDIX E

VHDL code for CPLD.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use ieee.numeric_std.all;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity VHDL_Module is

            Port (DAQ : in  STD_LOGIC_VECTOR (5 downto 0);    -- 6bit input address from DAQ
                  A : buffer STD_LOGIC_VECTOR (3 downto 0);  -- Stage 2 MUX of main board
                  B : buffer  STD_LOGIC_VECTOR (3 downto 0); -- Stage 2 MUX of exp board 1
                  C : buffer  STD_LOGIC_VECTOR (3 downto 0); -- Stage 2 MUX of exp board 2
                  D : buffer  STD_LOGIC_VECTOR (3 downto 0); -- Stage 2 MUX of exp board 3
                  E : out  STD_LOGIC_VECTOR (1 downto 0));   -- Stage 4

end VHDL_Module;

architecture Behavioral of VHDL_Module is
begin

process(DAQ)
begin

        case DAQ is
                when "000000" =>
                        E<="00"; A<="0000"; D<="0000"; B<="0000"; C<="0000";
                when "010000" =>
                        E<="01"; B<="0000"; A<="0001"; D<="0000"; C<="0000";
                when "100000" =>
                        E<="10"; C<="0000"; B<="0001"; A<="0001"; D<="0000";
                when "110000" =>
                        E<="11"; D<="0000";C<="0001"; A<="0001"; B<="0001";


                when "000001" =>
                        E<="00"; A<="0001"; D<="0001"; B<="0001"; C<="0001";
                when "010001" =>
                        E<="01"; B<="0001"; A<="0010"; D<="0001"; C<="0001";
                when "100001" =>
                        E<="10"; C<="0001"; B<="0010"; A<="0010"; D<="0001";
                when "110001" =>
                        E<="11";D<="0001";C<="0010"; A<="0010"; B<="0010";


                when "000010" =>
                        E<="00"; A<="0010"; D<="0010"; B<="0010"; C<="0010";
                when "010010" =>
                        E<="01"; B<="0010"; A<="0011"; D<="0010"; C<="0010";
                when "100010" =>
                        E<="10"; C<="0010"; B<="0011"; A<="0011"; D<="0010";
                when "110010" =>
                        E<="11"; D<="0010"; C<="0011"; A<="0011"; B<="0011";

                when "000011" =>
                        E<="00"; A<="0011"; D<="0011"; B<="0011"; C<="0011";
                when "010011" =>
                        E<="01"; B<="0011"; A<="0100"; D<="0011"; C<="0011";
                when "100011" =>
                        E<="10"; C<="0011"; B<="0100"; A<="0100"; D<="0011";
                when "110011" =>
                        E<="11"; D<="0011"; C<="0100"; A<="0100"; B<="0100";
```

```
when "000100" =>
       E<="00"; A<="0100"; D<="0100"; B<="0100"; C<="0100";
when "010100" =>
       E<="01"; B<="0100"; A<="0101"; D<="0100"; C<="0100";
when "100100" =>
       E<="10"; C<="0100"; B<="0101"; A<="0101"; D<="0100";
when "110100" =>
       E<="11"; D<="0100"; C<="0101"; A<="0101"; B<="0101";

when "000101" =>
       E<="00"; A<="0101"; D<="0101"; B<="0101"; C<="0101";
when "010101" =>
       E<="01"; B<="0101"; A<="0110"; D<="0101"; C<="0101";
when "100101" =>
       E<="10"; C<="0101"; B<="0110"; A<="0110"; D<="0101";
when "110101" =>
       E<="11"; D<="0101"; C<="0110"; A<="0110"; B<="0110";

when "000110" =>
       E<="00"; A<="0110"; D<="0110"; B<="0110"; C<="0110";
when "010110" =>
       E<="01"; B<="0110"; A<="0111"; D<="0110"; C<="0110";
when "100110" =>
       E<="10"; C<="0110"; B<="0111"; A<="0111"; D<="0110";
when "110110" =>
       E<="11"; D<="0110"; C<="0111"; A<="0111"; B<="0111";

when "000111" =>
       E<="00"; A<="0111"; D<="0111"; B<="0111"; C<="0111";
when "010111" =>
       E<="01"; B<="0111"; A<="1000"; D<="0111"; C<="0111";
when "100111" =>
       E<="10"; C<="0111"; B<="1000"; A<="1000"; D<="0111";
when "110111" =>
       E<="11"; D<="0111"; C<="1000"; A<="1000"; B<="1000";

when "001000" =>
       E<="00"; A<="1000"; D<="1000"; B<="1000"; C<="1000";
when "011000" =>
       E<="01"; B<="1000"; A<="1001"; D<="1000"; C<="1000";
when "101000" =>
       E<="10"; C<="1000"; B<="1001"; A<="1001"; D<="1000";
when "111000" =>
       E<="11"; D<="1000"; C<="1001"; A<="1001"; B<="1001";

when "001001" =>
       E<="00"; A<="1001"; D<="1001"; B<="1001"; C<="1001";
when "011001" =>
       E<="01"; B<="1001"; A<="1010"; D<="1001"; C<="1001";
when "101001" =>
       E<="10"; C<="1001"; B<="1010"; A<="1010"; D<="1001";
when "111001" =>
       E<="11"; D<="1001"; C<="1010"; A<="1010"; B<="1010";

when "001010" =>
       E<="00"; A<="1010"; D<="1010"; B<="1010"; C<="1010";
when "011010" =>
       E<="01"; B<="1010"; A<="1011"; D<="1010"; C<="1010";
when "101010" =>
       E<="10"; C<="1010"; B<="1011"; A<="1011"; D<="1010";
when "111010" =>
       E<="11"; D<="1010"; C<="1011"; A<="1011"; B<="1011";

when "001011" =>
       E<="00"; A<="1011"; D<="1011"; B<="1011"; C<="1011";
when "011011" =>
       E<="01"; B<="1011"; A<="1100"; D<="1011"; C<="1011";
when "101011" =>
       E<="10"; C<="1011"; B<="1100"; A<="1100"; D<="1011";
when "111011" =>
       E<="11"; D<="1011"; C<="1100"; A<="1100"; B<="1100";

when "001100" =>
       E<="00"; A<="1100"; D<="1100"; B<="1100"; C<="1100";
when "011100" =>
       E<="01"; B<="1100"; A<="1101"; D<="1100"; C<="1100";
```

```
                when "101100" =>
                        E<="10"; C<="1100"; B<="1101"; A<="1101"; D<="1100";
                when "111100" =>
                        E<="11"; D<="1100"; C<="1101"; A<="1101"; B<="1101";

                when "001101" =>
                        E<="00"; A<="1101"; D<="1101"; B<="1101"; C<="1101";
                when "011101" =>
                        E<="01"; B<="1101"; A<="1110"; D<="1101"; C<="1101";
                when "101101" =>
                        E<="10"; C<="1101"; B<="1110"; A<="1110"; D<="1101";
                when "111101" =>
                        E<="11"; D<="1101"; C<="1110"; A<="1110"; B<="1110";

                when "001110" =>
                        E<="00"; A<="1110"; D<="1110"; B<="1110"; C<="1110";
                when "011110" =>
                        E<="01"; B<="1110"; A<="1111"; D<="1110"; C<="1110";
                when "101110" =>
                        E<="10"; C<="1110"; B<="1111"; A<="1111"; D<="1110";
                when "111110" =>
                        E<="11"; D<="1110"; C<="1111"; A<="1111"; B<="1111";

                when "001111" =>
                        E<="00"; A<="1111"; D<="1111"; B<="1111"; C<="1111";
                when "011111" =>
                        E<="01"; B<="1111"; A<="0000"; D<="1111"; C<="1111";
                when "101111" =>
                        E<="10"; C<="1111"; B<="0000"; A<="0000"; D<="1111";
                when "111111" =>
                        E<="11"; D<="1111"; C<="0000"; A<="0000"; B<="0000";

                when others=>
                        null;

        end case;

end process;

end Behavioral;
```