Design of A Discrete 64 Channel Nerve Recorder

W. K. Hon

***Abstract*—Injuries which lead to the damage of the peripheral nerve can result in loss of motor function or sensory feedback. In severe cases, the damaged nerves do not regenerate leading to permanent disability. A possible solution lies in creating a neural link between the nerve and muscle thus bypassing the damaged portions totally. Such a system would require the recording, conditioning and interpreting of action potentials from the nerve sites using special electrodes. The objective of this project is to design and implement a 64-channel peripheral nerve recording system using discrete components. A novel design using a more efficient multiplexing algorithm was used to reduce the size, cost and power consumption of the system while still being able to provide a bandwidth of 30 kHz per recording channel. The drawback of the design is a degraded CMRR of 37.4dB at 50 Hz. To make up for the poor CMRR, a more aggressive low frequency cut off was adopted. Finally, an input referred noise of 2μVrms for each channel was achieved by the use of low noise amplifiers. The bandwidth for each channel was shown to be from 1 kHz to 10 kHz with a peak gain of 59.25dB at 3 kHz. The power requirement for a full 64 channel system as estimated to be 1.356W.**

I. INTRODUCTION

THE peripheral nervous system (PNS) is a collection of neuronal cells whose cell bodies are located in the spine and whose axons extend through peripheral nerves and terminate in certain sensory receptors or in neuromuscular junctions [1]. The PNS interfaces the central nervous system (CNS) to the skeletal muscles and sense receptors by transmitting information from sensory receptors to the CNS for sensing and transmitting information from the CNS to the skeletal muscles for reacting.

Such information is transmitted via electrochemical processes along a cable-like bundle of axons called the nerve. The peripheral nerve consists of both sensory and motor axons which are grouped into fascicles by an insulating perineurium; several fascicles are grouped together and surrounded by an insulating epineurium to form the peripheral nerve. It should be noted that neurons even within fascicles are grouped not according to their function (motor or sensory), but according to their destination. As one moves towards the spine, fascicles tend to fuse. Therefore, it is not possible to record or recruit fascicles based on their function [2].

Injuries which lead to the damage of the peripheral nerve can result in loss of motor function or sensory feedback. In severe cases, the damaged nerves do not regenerate leading to permanent disability. A possible solution lies in creating a neural link between the nerve and muscle and bypassing the damaged portions totally. Such a system would require the recording, conditioning and interpreting of action potentials from the nerve sites.

W. K. Hon is currently fulfilling his requirements for a Degree of Bachelor of Engineering with the Electrical Engineering Department, National University of Singapore.

II. OBJECTIVES

This paper describes the design and implementation of a discrete 64 channel nerve recording system. Fig. 1 shows the how the nerve recorder interfaces with the data acquisition unit.

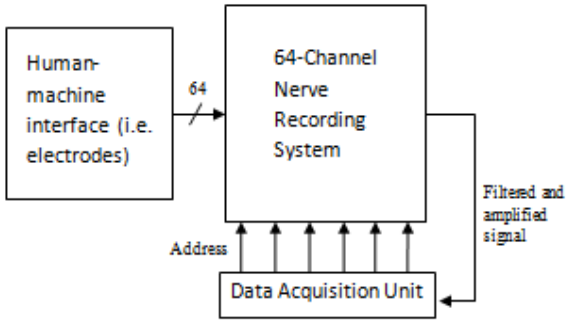


Fig. 1. Block diagram of the 64 channel nerve recording system and its interfaces.

Essentially, the data acquisition unit (DAQ) requests 1 of 64 channels through a 6-bit address supplied to the recorder, the recorder responds by supplying the DAQ with the correct filtered, differenced and amplified signal. The software running behind the DAQ is then able to separate the single stream of data back into their respective 64 channels; this can then be displayed or interpreted. Fig. 2 shows the main board of the recording system.

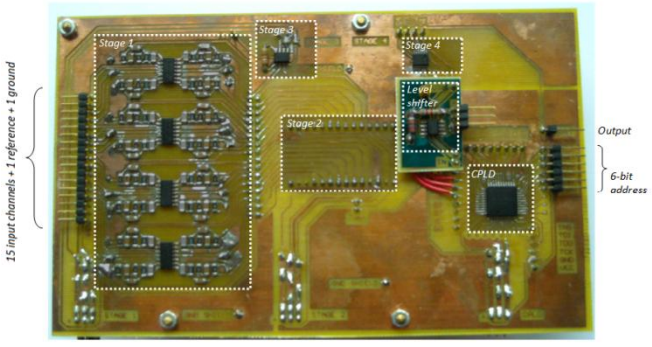


Fig. 2. Main board of the recording system. 16 channels are shown, additional expansion boards can be stacked to provide the other 48 channels.

III. Signals and Electrodes

The recording system is designed for a transversely implanted multichannel silicon electrode array, this is an intrafascicular type electrode and belongs to a class of intraneural penetrating electrodes [3]. Compared to widely used extraneural cuff electrodes which can only record compound action potentials (CAPs) due to its physical placement around the nerve, intrafascicular electrodes penetrate into the fascicles of the nerve allowing their active sites to be located in the space between axons, thus they are able to measure the activity from a single axon unit [3] [4]. When recording, a higher S/N ratio is achieved compared to extraneural electrodes [3]. The drawbacks however are its recording stability, biocompatibility and robustness [3], also it can cause nerve damage during the insertion process [4]. It should be noted that electrodes of this nature tend to have high impedances (up to 3 MΩ) depending on the size of the recording sites [5]. Fig. 3 shows the insertion of an A-style multichannel silicon electrode array from NeuroNexus into the sciatic nerve of a rat during a recording experiment.

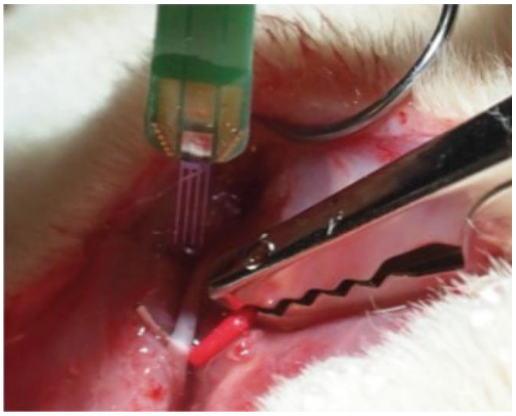


Fig. 3. Insertion of an A-style multichannel silicon electrode array from NeuroNexus into the sciatic nerve of a rat.

The bandwidth of the action potentials measured using intrafascicular type electrodes range from 1-10 kHz. Fig. 3 shows the bandwidth of the nerve signals measured using longitudinal intrafascicular electrode (LIFEs).

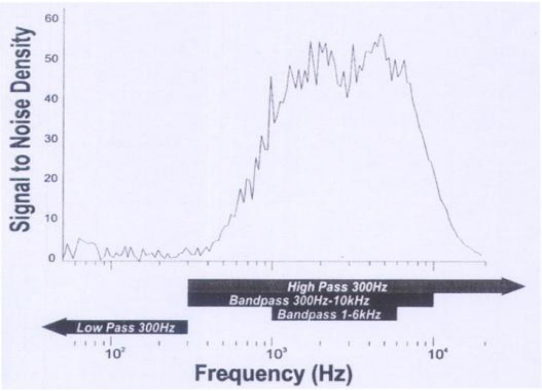


Fig. 3. Bandwidth of the neural signal represented by the signal to noise spectrum of the LIFE recording [6].

The magnitude of the nerve signals measured using intrafascicular electrodes is in the range of 200 – 350 µVpp [7].

IV. Design

Fig. 4 (see Appendix) shows the block diagram of the full 64-channel recording system. The following sub-sections describe the implementation of the various stages.

A. Analog Stage

The analog portions of the design comprise of stages 1 and 3. Fig. 5 shows the schematic of the two stages combined. Stage 1 pre-amplifies the signal by a gain of 20 and filters it from 1 kHz to 10 kHz (-3dB). Stage 3 amplifies the signal by a gain of 50 and also performs a differencing function to cancel out 50Hz line noise and any movement or physiological artifacts.

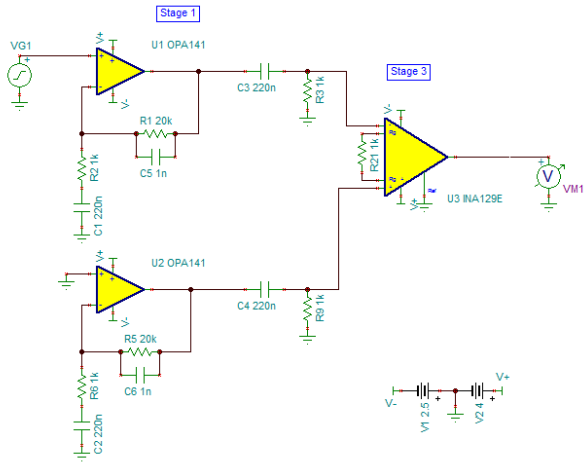


Fig. 5. TINA SPICE schematic of analog stages 1 and 3.

B. Multiplexing Algorithm

The stages involved in implementing the multiplexing algorithm are stages 2, 4 and the Programmable Logic Device (PLD). The PLD decodes the 6-bit address requested by the DAQ into four 4-bit addresses for each stage 2 multiplexer and one 2-bit address for the stage 4 multiplexer.

It should be noted that a simple switch and read mechanism would not work due to the design of the system. This is because stage 3 is being multiplexed into, thus a short amount of time is required for the output of stage 3 to settle before switching stage 4 to read the value. The settling time for a stage 3 amplifier is slightly above 1 µs, this sets the sampling rate limit of 1 MHz for a simple switch and read mechanism. To increase the maximum sampling rate, a preemptive multiplexing algorithm is used to allow for more time for the signals in stage 3 to settle before stage 4 multiplexes it to the DAQ.

The algorithm is as follows (refer to Fig. 4 in Appendix):

1. On start up, channel 1:1, 2:1, 3:1 and 4:1 are selected by stage 2 and are already settled
2. Stage 4 reads channel 1:1
3. Stage 4 reads channel 2:1. Stage 2 switches channel 1:1 to 1:2
4. Stage 4 reads channel 3:1. Stage 2 switches channel 2:1 to 2:2
5. Stage 4 reads channel 4:1. Stage 2 switches channel 3:1 to 3:2
6. Stage 4 reads channel 1:2. Stage 2 switches channel 4:1 to 4:2
7. Stage 4 reads channel 2:2. Stage 2 switches channel 1:2 to 1:3
8. Stage 4 reads channel 3:2. Stage 2 switches channel 2:2 to 2:3
9. Stage 4 reads channel 4:2. Stage 2 switches channel 3:2 to 3:3
10. Stage 4 reads channel 1:3. Stage 2 switches channel 4:2 to 4:3
11. Continue

In effect, this algorithm preempts the next address and switches first so that when the actual address arrives, no switching of stage 2 into the difference amplifier is required thus extending the allowable settling time for each stage 3 amplifier to 3µs

Fig. 6 shows how the algorithm works on the actual system, note that the maximum switching frequency of the DAQ is 1 MHz. Here, three signals are shown, input address change from DAQ (top), output of stage 3 (center) and output of stage 4 (bottom). It can be seen that when the address changes, it takes about 1µs for the output of stage 3 to settle, this is due to the rise time incurred when stage 2 multiplexes into the stage 3 amplifier. After 3µs from address change, stage 4 switches the output of stage 3 to the DAQ, by this time the signal is already well settled. Note that an extra leeway of 2µs is left which will allow the switching frequency to go up to 2 MHz, or 31250 Hz per channel.

Fig. 6. Signals at three different stages showing the function of the multiplexing algorithm. Input address change from DAQ (top), output of stage 3 (center) and output of stage 4 (bottom).

C. Choice of Components

For the front end amplifiers in stage 1, the OPA4141 by Texas Instruments was chosen due to its low voltage noise of $6.5\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$ from 1-10 kHz and low current noise of $0.8\ \mathrm{fA}/\sqrt{\mathrm{Hz}}$ at 1 kHz. A low current noise is important as the impedances of multichannel silicon electrodes can reach values up to 3MΩ [5] due to the small electrode sites.

An instrumentation amplifier was chosen for stage 3 because the high input impedance buffers the filtering components at the input. The INA129 by Texas Instruments was chosen as it has the fastest settling time in its category, this is important because the amplifier is being multiplexed into when address change occur, the settling time will thus limit the maximum achievable data acquisition rate.

The ADG706 and ADG604 were chosen as the multiplexers for stage 2 and stage 4 respectively. Both boast a very low power consumption of less than 0.01µW. The ADG604 was chosen specifically for its low input capacitance of 18 pF. A low input capacitance prevents charge build up and reduces crosstalk during switching.

The XC2C32A CoolRunner-II CPLD by Xilinx was chosen as the programmable logic platform, it has a minimal logic delay of 3.8ns which reduces time delay between actual address input and correct signal output. A total of 18 outputs (4 for each stage 2 multiplexer and 2 for the stage 4 multiplexer) and 6 inputs (6-bit address from DAQ) were required, this is supported by the 33 user IOs of the CPLD.

V. Main Results

A. Frequency and Phase Response

Fig. 7 shows the frequency and phase response obtained with a spectrum analyzer. The bandwidth of a channel was shown to be from 1 kHz to 10 kHz with a peak gain of 59.25dB at 3 kHz and is stable over all frequencies.

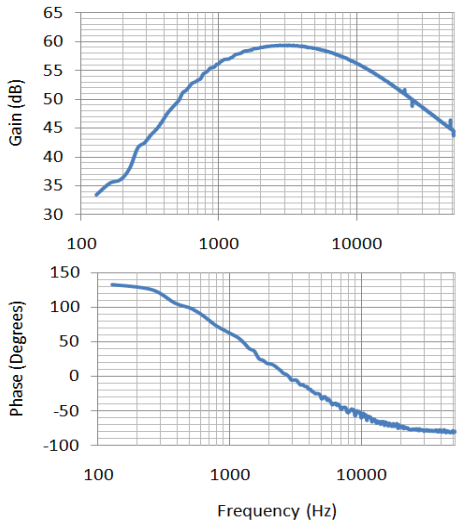
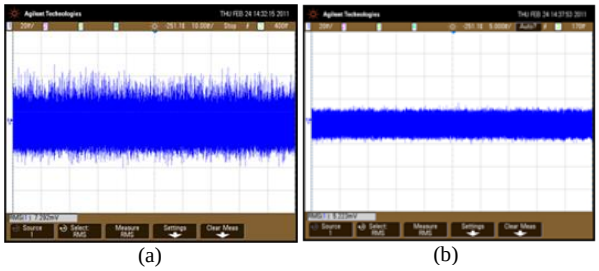


Fig. 7. Bode plot of a single channel obtained from a spectrum analyzer

B. *Noise*

The system noise was estimated by measuring the RMS noise at the output when the input channel is grounded and then subtracting this value by the oscilloscope's noise. The value is then referred to the input by a division of 1000. An input referred noise of 2 µVrms was obtained. Fig. 8 shows (a) the noise measured at the system output (b) and by shorting the probe connectors together.

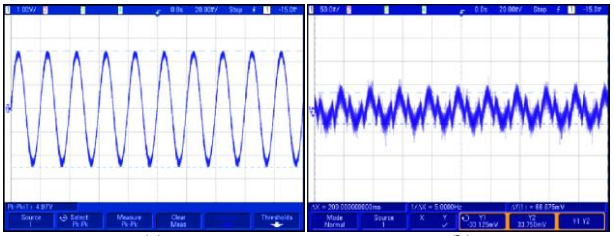


(a) (b)

Fig. 8. (a) Showing an output noise of 7.2 mVrms, measured at the system output. (b) Showing an oscilloscope noise of 5.223mVrms measured by shorting probe connectors together.

C. *CMRR at 50 Hz*

To calculate the CMRR, a 700mVpp, 50 Hz, test signal was connected to one input channel and the reference was connected to ground to obtain the differential mode gain. Fig. 9 shows (a) the output sine wave at 4.97Vpp. To obtain the common mode gain, both the reference and input were connected to the test signal. Fig. 9 shows (b) the output voltage of 66.87mVpp, in common mode. This results in a CMRR of 37.4 dB at 50 Hz. The poor CMRR is due to the addition of passive components between the gain and differencing stages.



(a) (b)

Fig. 9. (a) Showing an output noise of 7.2 mVrms, measured at the system output. (b) Showing an oscilloscope noise of 5.223mVrms measured by shorting probe connectors together.

D. *Software De-multiplexing*

The multiplexed signal at the output of stage 4 (see Fig. 4 in Appendix) is fed into the DAQ where it is de-multiplexed in software back into the respective 64 channels. To interface the dual supply recording module to the single supply DAQ, the DAQ inputs were referenced to a -2.5V source tapped from the recording module. Fig. 10 shows the software de-multiplexed waveform graphs of 16 channels. Each graph displays up to 8 individual channels. It can be seen that the software successfully displays a 1 kHz, 2mVpp sine wave at one of the input channels.

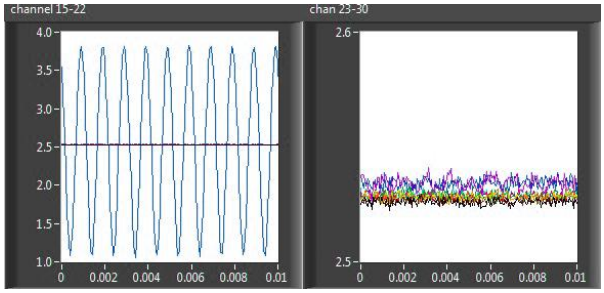


Fig. 10. Software de-multiplexed waveform graphs of 16 channels (8 channels per graph). One channel was given an input sine wave at 1 kHz, 2mVpp.

VI. System Specifications

The system specifications are summarized in Table I below.

TABLE I
SUMMARY OF SYSTEM SPECIFICATIONS

Gain	59.25dB at 3kHz
Bandwidth (-3dB)	1kHz to 10kHz
Noise (RTI)	2µVrms
CMRR (at 50Hz)	37.4dB
Maximum sampling rate per channel	31250 Hz
Power consumption (estimated for 64 channels)	1.356W

VII. Conclusion

In conclusion, the proposed design provides an efficient way to implement a multi channel discrete system for test and measurement in a laboratory environment. However, due to its size and power consumption it is infeasible for any kind of chronic experiments.

One advantage of the proposed design is that the maximum sampling rate scales with the total number of channels needed, thus the number of channels can be increased while maintaining the same bandwidth for each channel. Another advantage of such a design is the ability to conserve power by reducing the number of high gain amplifiers.

Even though the discrete system is not suitable for implants, the same switching algorithm can be applied to integrated solutions to reduce both area and power.

APPENDIX

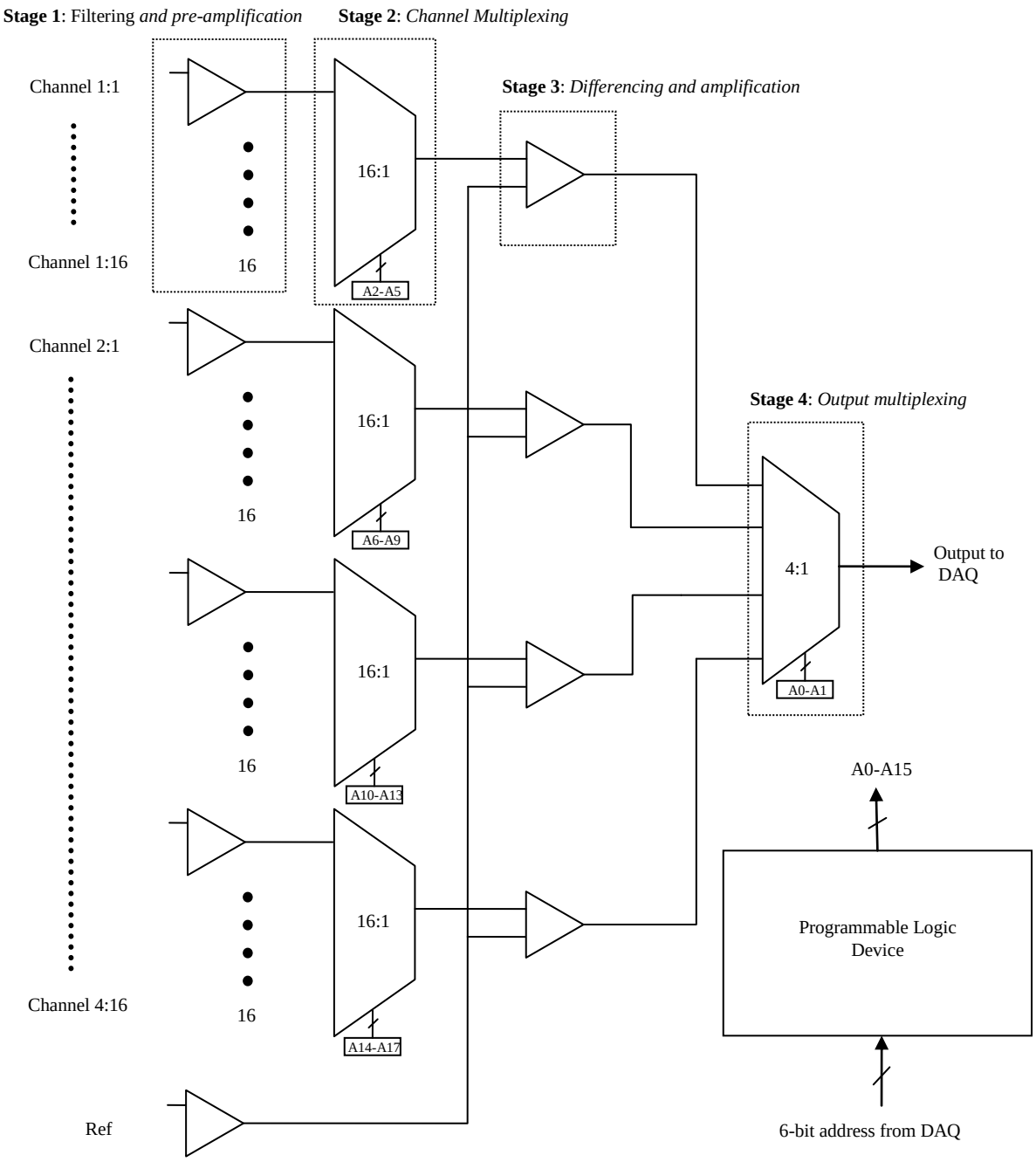


Fig. 4. Block diagram of the full 64 channel recording system model.

ACKNOWLEDGMENT

I would like to thank my two supervisors, Associate Professor Xu Yong Ping and Associate Professor Yen Shih Cheng for their patience and guidance throughout the project. Also, I would especially like to thank Ng Kian Ann for his invaluable help, advice on the multiplexing algorithm and many other areas.

REFERENCES

[1] Navarro, X., et al., *A critical review of interfaces with the peripheral nervous system for the control of neuroprostheses and hybrid bionic systems.* Journal of the Peripheral Nervous System, 2005. **10**(3): p. 229-258.

[2] Horch, K.W. and P.R. Burgess, *Peripheral Nervous System*, in *Neuroprosthetics Theory and Practice*, K.W. Horch and G.S. Dhillon, Editors. 2004, World Scientific.

[3] Yoshida, K. and R. Riso, *Peripheral Nerve Recoding Electrodes and Techniques*, in *Neuroprostheses Theory and Practice*, K.W. Horch and G.S. Dhillon, Editors. 2004, World Scientific.

[4] Branner, A. and R.A. Normann, *A multielectrode array for intrafascicular recording and stimulation in sciatic nerve of cats.* Brain Research Bulletin, 2000. **51**(4): p. 293-306.

[5] *NeuroNexus Technologies*. [cited 2011; Available from: http://www.neuronexustech.com/Portals/0/Catalog%20&%20Manual/catalog_june09.pdf.

[6] Yoshida, K. and J. Struijk, *The Theory of Peripheral Nerve Recording*, in *Neuroprosthetics theory and Practice*, K.W. Horch and G.S. Dhillon, Editors. 2004, World Scientific.

[7] Jia, X., et al. *AAHS Session B3: Congenital and Nerve II*. in *American Association for Hand Surgery 2010 Annual Meeting*. 2010.